Most Significant Bits

HP Pushes PA-7100LC to 100 MHz

Taking advantage of its PA-7100LC processor to reduce system cost, HP has introduced a new line of workstations with entry system prices between $10,000 and $20,000. The new Model 715 systems offer more features and more expandability than the previously announced Model 712 systems *(see **080103.PDF**)* and, for the first time, include a 7100LC processor running at 100 MHz. At its new clock speed, the 7100LC delivers 101 SPECint92 and 137 SPECfp92.

As the latter number shows, HP has removed the fetters from the 7100LC's floating-point unit, allowing the chip to show its full performance potential. The earlier Model 712/80i was artificially restricted to 79 SPECfp92; that system has been replaced by the 712/80, which delivers 121 SPECfp92 at the same price.

The 7100LC offers far better FP performance than Sun's MicroSparc-2, and the new 100-MHz version outruns the fastest SuperSparc chip, which is rated at 89 SPECint92 and 103 SPECfp92, by a significant margin. Using parallel subword arithmetic *(see **080103.PDF**)*, the 100-MHz chip can decode MPEG-1 video at the full 30 frames per second with stereo audio.

The fastest of the new systems, which are all shipping now, is the 715/100, carrying a $19,000 list price with 32M of memory, a 525M disk, and a 17" color monitor. The 64- and 80-MHz versions, however, offer about the same integer performance as 66- and 90-MHz Pentium PCs for about twice the price of the PC, making the HP systems attractive mainly to users that need the extra floating-point speed or the MPEG decoding ability.

PowerPC 603 Aggressively Priced

Motorola rolled out surprisingly low prices for the PowerPC 603 processor, sampling now and due to ship next quarter. The company will sell the 66-MHz 603 for $160 in quantities of 20,000, while the 80-MHz version lists for $199 in similar quantities. Applying our normal 25% adjustment, we estimate that 1,000-piece pricing will be $200 and $250, respectively. IBM has not yet announced 603 pricing but expects to have "similar" prices.

Motorola is motivated to offer low prices on the 603 to shift buyers away from the 601, as the company builds the 603 itself but must purchase 601 chips from IBM for resale. The new prices are below that of Intel's 486DX-33, a chip with one-third the performance of the 80-MHz 603 and a list price of $260 in 1,000-unit quantities. In fact, Intel does not have a single processor with a floating-point unit at a lower list price than the 603's.

Even at these prices, Motorola can make money: the MPR Cost Model *(see **071004.PDF**)* estimates the manufacturing cost of a 603 at $50, about the same as a DX4 and a few dollars more than a DX2. The 20,000-piece price is somewhat meaningless in any case, as only one customer is currently purchasing PowerPC chips in that quantity, and Apple isn't paying list price.

IBM Phasing Out POWER Architecture

While expanding its RS/6000 line, IBM indicated that its POWER architecture will be phased out in favor of PowerPC, possibly as early as next year. The new product rollout features PowerPC-based workstations at the low end coupled with high-end systems using a low-cost version of Power2. Over the next year, these Power2 systems will be replaced by products using faster PowerPC 604 and 620 chips. The multichip follow-on to Power2 is now being called the PowerPC 630.

The new Model 41T uses the 80-MHz PowerPC 601 to achieve 79 SPECint92 and 90 SPECfp92 without an external cache. With the optional $1,500 512K cache, the system reaches 88 SPECint92 and 99 SPECfp92, exceeding expectations on the integer side but not for FP. This product uses a half-speed (40-MHz) processor bus. The base system price is $11,200 (without cache), giving the 41T price/performance comparable to HP's new Model 715 line. As with HP's workstations, the IBM system can be matched in integer performance by a comparably configured Pentium PC selling for half the price.

As we predicted *(see **071301.PDF**)*, IBM has reduced the cost of its multichip Power2 processor to make it suitable for desktop systems starting at $29,500. The new "Power2–" version uses ball-grid array (BGA) packaging *(see **071203.PDF**)* instead of the costly multichip module (MCM) package used in the server model. It also eliminates two cache chips, reducing the size of the data cache to 128K. The discrete packaging forces a slight reduction in clock speed from 71.5 to 67 MHz.

The reduction in cache size and clock rate causes a 20% drop in performance, to 101 SPECint92 and 201 SPECfp92. For some large scientific applications, the effect is even more severe; to alleviate this problem, IBM added an optional second-level cache to Power2–. The new ICU chip generates control signals for this cache, which sits on the main memory bus and can be as large as 1M. The second-level cache, however, does little to improve SPEC ratings. Systems using Power2–, as well as the 601-based boxes, are now available.

IBM expects that the PowerPC 620 will have taped out by the time you read this; volume shipments are planned for 2Q95. The company is also investigating enhancements to the Power2 processor, but the lower cost and better performance of the 620 will probably convince Big Blue not to bother extending Power2.

What used to be Power3 is now the PowerPC 630. It

remains a multichip design similar to Power2, intended for maximum performance without being constrained by standard packaging or voltages. IBM is developing the 630 independently of Somerset but plans to sell the chip set through its Microelectronics group. The company says that it will offer the design to partner Motorola as well, which may choose to sell the device but probably won't bother to build it. While the 630 is the first new PowerPC design to be revealed in nearly three years, IBM hopes to provide additional details about 603/604/620 follow-ons in the next few months.

Digital Recompiles into Performance Lead

In another of a series of escalating claims, Digital has announced new performance numbers for its 21064 systems that exceed those of HP's high-end 125-MHz 7150 *(see **0805MSB.PDF**)* just as HP is beginning to ship systems using its fastest chip. The new results (achieved on existing systems with new compilers) show 138 SPECint92, about 2% better than the HP processor.

Digital hopes to make this performance competition moot with the release of its 275-MHz 21064A, which the company expects to achieve about 170 SPECint92 and 290 SPECfp92. Carrera Computers (Laguna Hills, Calif.) and Aspen Systems (Wheat Ridge, Col.) have already announced boxes using this processor, with systems running OSF/1 and Windows NT expected to ship this fall. Carrera says that its Cobra AXP 275 will start at $7,995, while Aspen declined to name a price.

Also according to Digital, the 21066 has begun to ship in volume. Originally due in 1Q94, functional problems have slowed its release. Digital, however, has yet to announce a 21066-based system, and no third parties appear to be shipping 21066 systems, although a few have been announced. Thus, it isn't clear to whom the 21066 is shipping in volume. The 70-SPECint92 chip doesn't seem to fit Digital's current Alpha positioning, which emphasizes better-than-Pentium performance.

In a related announcement, U.K. notebook maker Tadpole says that it will develop a 21066-based portable system to go along with its popular SPARC notebooks and forthcoming portable PowerPC system. Tadpole did not specify a shipment date for its Alpha product.

Digital is also the first company to reveal baseline SPEC results for its systems. These tests use the same benchmarks as the normal SPEC suite, but certain compiler optimizations are disallowed *(see **0803MSB.PDF**)*. These results show that, even with baseline optimization, the 21064 achieves 130 SPECint92, 6% lower than the fully optimized result. SPECfp92 shows a degradation of just 5%. Among the individual benchmarks, only *li*, *ear*, *swm256*, and *fpppp* show greater than a 10% reduction, and none is affected by more than 20%. These results show that Digital's processors and compilers achieve high marks without requiring excessive tuning; the challenge now is for other vendors to show the same ability.

Hitachi Licenses PowerPC from IBM

Two former enemies buried the hatchet as Hitachi signed an agreement to license technology from IBM that allows it to build POWER and PowerPC systems. The two companies had been bitter mainframe rivals in the '80s, when Hitachi was accused of stealing secrets from IBM, but with the mainframe market dwindling, the two have decided to share technology. In addition to 3090-compatible mainframes, Hitachi plans to build systems compatible with IBM's SP series of massively parallel (MPP) systems, which currently use POWER processors. Hitachi is investigating the option of building personal computers using PowerPC chips.

Hitachi is also a charter member of HP's Precision RISC Organization. A senior Hitachi executive states that the IBM deal does not threaten Hitachi's commitment to HP's RISC architecture. The Japanese vendor is currently focusing its PA-RISC efforts on two areas: UNIX-based workstations/servers and embedded applications. IBM's RISC processors will be used in high-end systems and potentially in PCs. The only conflict seems to be in the MPP area, where Hitachi has been working on a PA-RISC system. The company's interest in the SP series may be due to IBM's rumored plans to port its mainframe operating system to that platform.

Even so, the deal must make HP nervous, as it positions Hitachi to make a complete jump to PowerPC if that architecture's popularity increases.

VLSI ARMed for Smart Peripherals

Aiming for design wins in smart peripherals and portable devices, VLSI has announced the Ruby processor, which combines an ARM6 core with PCMCIA (slave only), ISA, serial, and parallel interfaces. The new device operates at speeds up to 30 MHz and will be priced at around $30 when production begins this fall.

Ruby's host interface contains 8 data lines, 12 address lines, and control signals for both PCMCIA and ISA, so it can be used for expansion cards implementing either standard. The chip includes the usual 32-bit ARM bus for connecting to external memory, although software can also take advantage of the 2K on-chip SRAM.

Ruby has an 8-bit parallel port as well as low-speed (asynchronous) and high-speed (synchronous) serial ports. These ports can transfer data to standard communications devices, such as modems, and other peripheral chips. Finally, Ruby has its own timers and interrupt controller, reducing the need for external system logic.

The chip runs at 2.7–5.5 V, making it well-suited to battery operation. Power usage is typically 200 mW at 5 V (30 MHz) and a miserly 110 mW at 3.3 V (25 MHz). Standby and sleep modes further ease power consump-

tion. The high level of integration reduces system power as well as size and cost. The list price is $31.90 in a 176-pin TQFP or $30.00 in a 144-pin TQFP; the latter version restricts the ARM bus to 8 bits instead of 32.

This announcement continues VLSI's rapid deployment of embedded ARM chips *(see **0805MSB.PDF**)*. The new device offers a powerful controller for add-in modem, wireless LAN, and other communications cards. It can also serve as the CPU in portable telephones and similar devices, although without an MMU it is not suitable for PDAs. The ARM chip offers better performance than similarly priced 683xx processors, which currently dominate this market segment. The Motorola chips still lead in development tools and other infrastructure.

Motorola Launches FlexCore Program

Seeking to capitalize on its dominance of the embedded market, Motorola has unveiled an aggressive custom-processor program called FlexCore to formalize (and commercialize) a policy the company has been using for years: find volume customers that want to integrate 68000-family cores into application-specific chips, sell them tools and access to manufacturing capabilities, and incorporate the resulting product into the Motorola product line. The FlexCore program targets customers that have proprietary technology, high volume, or both.

Motorola will provide processor cores as well as peripherals and interfaces from its standard-cell library and the option to integrate custom logic. There is also potential for FlexCore devices to become a standard Motorola product, if the customer and Motorola both agree to do so. This arrangement would allow the development costs to be spread over additional units.

To take advantage of the program, customers must design using the standard-cell process and deliver a netlist to Motorola. Motorola then performs layout, verification, fabrication, and testing. The company claims that it can deliver silicon as early as three months after receiving the customer's design. The program currently supports Cadence tools for schematic capture, synthesis, and simulation. Hardware-emulation tools for FlexCore devices are available from Orion Instruments (Menlo Park, Calif.). Motorola charges a typical NRE fee of $125,000. An example design comprising a 68EC000 core, a SCSI controller, 512 bytes of RAM, and 15,000 gates of logic would cost about $15 per chip.

The first processor cores available are based on the 68EC000 and 68020, delivering 3 and 8 Dhrystone MIPS, respectively. A 68030 core rated at 12 MIPS will be available in late 1994, followed by the 36-MIPS 68040 in mid-1995 and 68060 and PowerPC cores late in 1995. All the cores are fully static designs that can run at either 5 V or 3.3 V. To go with the processor cores, Motorola is offering its standard cell library of 150 design elements. All are designed for a 0.65-micron CMOS process.

One example of a FlexCore product is the 68322, developed with Peerless Systems (El Segundo, Calif.) for low-cost laser printers *(see **080604.PDF**)*. SunDisk (Santa Clara, Calif.) used FlexCore to build a proprietary controller chip for its PCMCIA flash-memory card. The controller incorporates an EC000 core, sequencer, and datapath and error-correction circuitry. The chip will not be sold on the open market but will be used only in SunDisk's product.

FlexCore is similar to the CoreWare program announced by LSI Logic a couple of years ago *(see **0603MSB.PDF**)*. LSI's library of cores and particularly peripherals is not as extensive as Motorola's. LSI is currently shipping samples of its LR33300 and LR33310 processors *(see **071703.PDF**)*, built in the 0.6-micron CoreWare process, and is scheduled to move to a 0.5-micron process mid-1994.

As embedded systems continue to shrink and adopt the system-on-a-chip approach, a modular core program is essential to meeting customer design objectives. Motorola has managed to keep its lead in the embedded market by producing a wide range of application-specific designs, but the new program allows the company to match its chips to a particular customer. This adaptability will help keep the 68K in the catbird's seat.

SPARC Becomes IEEE Standard

After a four-year battle, Sun has successfully convinced the IEEE Computer Society to adopt SPARC as an official standard, now dubbed number 1754-1994. The standard is an extension of SPARC version 8 and is the first microprocessor architecture standard adopted by the IEEE. Many non-SPARC processor vendors had objected to the standard, but the IEEE was convinced by the large installed base and open availability of the architecture.

Sun wasted no time in announcing that its products are compatible with IEEE 1754. It hopes to convince system buyers that an industry-standard architecture is an essential checklist item. The benefits of this standard to the buyer (or anyone else) are unclear, as the architecture has long been available for a minimal licensing fee. But the number of SPARC processor vendors has been dwindling, not increasing—particularly for general-purpose systems, this standardization is more of a gimmick than any real progress.

Embedded CPU vendors may find some value in using a free architecture rather than developing one from scratch. Fujitsu has been the only company to attempt to popularize SPARC in this area, so far with little success. Perhaps, as architectures go, you get what you pay for. ♦

