IBM Reveals Minimal PowerPC 401 Core

New Core Design Pushes PowerPC Down into Consumer Price Range

by Jim Turley

To boost the company's budding ASIC design program, IBM has developed the smallest PowerPC design yet, reducing the core to just 5.5 mm^2. The new design maintains full PowerPC software compatibility but lowers IBM's manufacturing costs, allowing it to pursue higher-volume consumer electronics designs.

IBM revealed the first details of the core at the Microprocessor Forum in October. The 401 reduces the conventional PowerPC five-stage pipeline to just three stages, affording IBM the opportunity to reduce the core's complexity, size, and cost. The new core is being offered as part of IBM's SystemCore ASIC-development program and is aimed at high-volume applications in communications and consumer electronics. The first 401-based designs are expected to debut in 1Q96. IBM's embedded roadmap also includes a higher-performance derivative, the 405, due in 1997.

Missing Features Shrink Die

The 401 is a smaller sibling to IBM's existing 403 embedded core. The 401 saves space by using a simple three-stage pipeline without an integrated multiply-divide unit, cache controller, MMU, or floating-point support.

A 32 × 32 → 32-bit integer multiply takes 19 clock cycles; 16 × 16-bit multiplies require only 11. In the absence of a dedicated multiply/divide unit, division is a fairly lengthy operation. The 401 calculates one bit per clock cycle, plus three clocks of overhead. Thus, a 32/32 → 32-bit division completes in 35 cycles. Loads and stores take two clocks, plus memory latency.

Table 1 compares the features of the 401 with other vendors' 32-bit embedded processor cores. The 401 core measures 5.5 mm^2, sans cache, in IBM's 0.44-micron three-layer-metal CMOS-5S process. This is about 50% larger than either the smallest MIPS-based core from LSI Logic or Cirrus Logic's ARM7 core. All three cores have minimalist three-stage pipelines, fixed-length 32-bit instructions, and no FP support.

The miniature PowerPC core is burdened somewhat by its heritage as a complex workstation CPU with a relatively rich instruction set. It appears that PowerPC cores will never be as small (and hence, inexpensive) as comparable 32-bit architectures. Even Digital's upcoming StrongArm core *(see **091504.PDF**)* is smaller than the 401, yet delivers 4–5× the performance.

Price & Availability

The PowerPC 401 core has been fabricated and will be available for customer designs in 1Q96 along with the first 401-based standard part. For more information, contact IBM Microelectronics (Research Triangle Park, North Carolina) at 800.769.3772 or access the IBM Web site at *www.chips.ibm.com.*

Uphill Climb Ahead for IBM

IBM's embedded PowerPC operation in North Carolina is independent of Somerset, the company's joint design effort with PowerPC partner Motorola. The organization is barely a year old and has not yet developed a broad repertoire of cores and peripheral modules. Consequently, IBM's first three embedded processors, the 403GA, 403GB, and 403GC, are nearly identical, differing mainly in an MMU and number of serial ports. Adding the 401 core will help IBM extend its roster and move beyond its narrow product line. The company also plans to leverage the numerous designs carried out at its far-flung development facilities around the country.

There are now multiple vendors in the embedded-core market, and the list is growing. NEC has added ARM to its arsenal in addition to a MIPS license and the proprietary V800 family. This combination of cores and NEC's extensive ASIC experience promise to make the company a major player in this market.

For its part, IBM is also pushing to become a major player in the burgeoning microprocessor-based ASIC market. The company has a long road ahead of it as it seeks to extend its peripheral library and core selection. IBM has gained valuable experience with its previous three designs, and the addition of the 401 core should attract a new group of customers. ♦

Vendor	IBM	LSI Logic	Cirrus	Digital
Core	401	CW4001	ARM7	StrongArm
Die Size	5.5 mm^2	3.5 mm^2	3.8 mm^2	3.8 mm^2
Process	0.44µ 3LM	0.5µ 2LM	0.7µ 3LM	0.35µ 3LM
Voltage	3.3 V	3.3 V	3.3 V	1.5 V
Max. freq	50 MHz	60 MHz	33 MHz	160 MHz
MIPS*	45 MIPS	45 MIPS	30 MIPS	185 MIPS
16 × 16 → 32	11 clks	13 clks	2–17 clks	2–17 clks
32 × 32 → 32	19 clks	13 clks	2–17 clks	2–17 clks
32 / 32 → 32	35 clks	36 clks	(software)	(software)

Table 1. IBM's 401 core is about 50% larger than comparable 32-bit CPU cores. *Based on Dhrystone 2.1 (Source: vendors)

