New 56301 DSP Doubles 24-Bit Performance

Motorola 56300 Core Upgrades 56000 Pipeline, Clock Speeds

by Jim Turley and Phil Lapsley

Motorola's new 56300 DSP family promises to double the performance of the company's popular 56000 product line, boosting the company into the high end of the digital-signal-processing market. The 56300 is the first significant new DSP architecture to be released by Motorola in several years.

The first chip in the family, the 56301, is aimed at multiline voice/data/fax processing and ATM equipment. Although the 56301 is the most powerful fixed-point DSP from any vendor to date, its steep price may restrict its success to a small niche of high-end products.

The 56300 family is Motorola's second generation of 24-bit DSP processors. The new core is binary compatible with the 56000 family and offers roughly twice its instruction execution rate. The new family has a redesigned pipeline, an improved data path with a 56-bit barrel shifter, and new instructions to take advantage of added features.

The 56300 family is the first sign of the reawakening of Motorola's DSP division, which was reorganized and promoted to the status of a corporate division last year, at which time a new management team was installed.

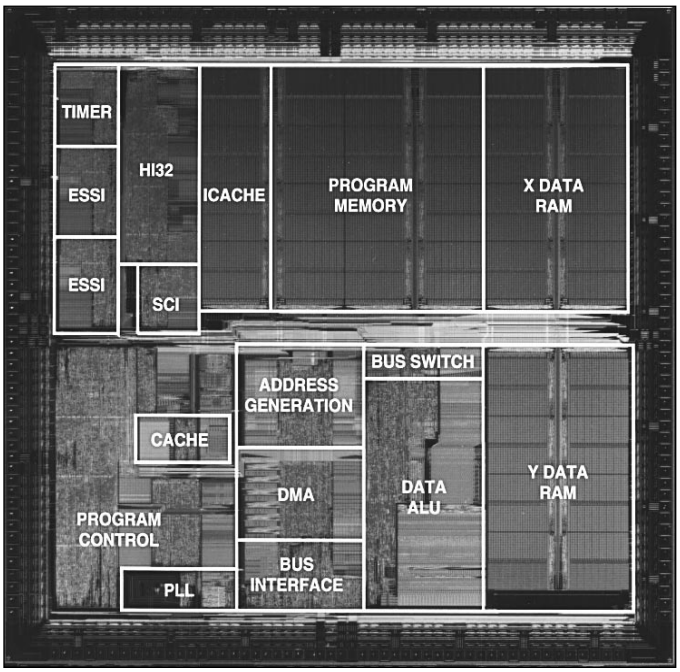


Figure 1. In Motorola's 0.5-micron three-layer-metal process, the 56301 measures about 7.6 mm on a side (58 mm^2). The new 56300 core accounts for only a small portion of the total die area.

Longer Pipeline Boosts Performance

Motorola achieved the speedup by going from a three-deep pipeline on the 56000 to a seven-deep pipeline on the 56300. In his presentation at October's Microprocessor Forum, Motorola Technical Manager Roman Robles described how the design team installed interlocks and other trickery to keep the pipeline compatible with the 56000, allowing the 56300 to execute existing 56000 binaries.

The longer pipeline allows the 56300 core to reach at least 66 MHz—significantly faster than most other DSPs—with 80-MHz parts expected in 1Q96. A 100-MHz version is also planned.

The 56300 executes all its instructions in a single clock cycle, another improvement over its predecessor. The redesigned ALU supports arithmetic saturation and two's-complement rounding, both common features, and 16-bit arithmetic, which is useful for calculating many algorithms originally designed for 16-bit DSPs.

The architecture's 24-bit instruction word means that the processor requires fewer instructions—compared to some 16-bit chips, significantly fewer—than many other DSPs to accomplish the same work. Combined with its faster clock rate, the processor's performance should be very good. However, it may also require more program memory due to the wider instruction word, increasing system cost.

Benchmark Results Look Encouraging

Although no empirical data is available yet, the 56300 is similar enough to the 56000 to draw some conclusions about the performance of the new design. On Berkeley Design Technology's DSP benchmarks, the 56000's total instruction cycle counts are about 22% lower than those of TI's TMS320C5x. The TI part has a maximum instruction execution speed of 50 MHz; thus, the 56300 wins on both clock speed and instruction-set efficiency.

TI's newer 320C54x has an improved instruction set that rivals the 56000 in terms of cycle counts. The C54x's normalized instruction cycle count is only about 3% greater than the 56000's but, like the C5x, it tops out at 50 MHz.

Conversely, the AT&T DSP1627, at 70 MHz, runs at about the same clock speed as the Motorola part, but its instruction set is considerably less efficient: the 56000's total normalized cycle count is about 30% better than that of the DSP1627 on the BDT benchmarks.

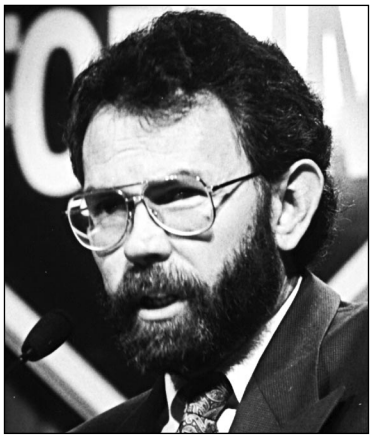
Overall, given the 56300's architectural improvements over the 56000 and its faster clock rate, it should take first place by a significant margin over all DSPs in the BDT benchmarks for execution speed.

56301 Designed for Expansion

Coincident with its architectural disclosure, Motorola announced the first chip in the 56300 family, the 56301. The company didn't skimp on features when designing the 56301. The part includes a number of sophisticated peripherals, including a DMA controller, PCI host interface, three timers, memory controller, and extra program memory that can be converted to an instruction cache.

The six-channel DMA controller has its own on-chip address and data buses, which keeps the DSP core from stalling unless there is contention with the DMA for the external bus. The DMA also supports a variety of transfer modes useful for image processing, like moving data between a frame buffer and memory.

The chip also carries a complete PCI host bus interface, which can be transformed into an ISA bus interface through software control. A quarter of the 301's external pins are devoted to the combination PCI/ISA interface's signals, though only a small proportion of the silicon is used by the bus-control logic.



MICHAEL MUSTACCHI

Motorola Technical Manager Roman Robles outlines his company's 56300 DSP design.

Geared for Special Applications

The 56301 is capable of tackling the most complex of applications for a single DSP. Although it carries 2K words each of X and Y data RAM and 3K words of program RAM, it also has a memory controller for glueless interfacing to DRAMs or to synchronous or asynchronous SRAMs. Most DSP applications don't reference external RAM very frequently and are not particularly sensitive to access times, so the DRAM controller adds unnecessary cost for many users. On the other hand, for developers tackling memory-intensive DSP applications, the on-board controller will save additional hardware development.

On top of its conventional program RAM, another 1,024 words of on-chip memory can be configured as either additional program RAM or as an eight-way set-associative instruction cache. Caches are usually anathema to DSP applications because of their nondeterministic performance. Again, this feature will be interesting mainly to developers of very large programs.

56301 Is an Expensive Start to the Family

The 56301 is shipping now at 66 MHz and sampling at 80 MHz. Motorola plans to ramp production of the 80-MHz parts in 1Q96, when it will begin sampling 100-MHz parts. The chip is available in either a 208-lead TQFP or a 252-contact plastic ball-grid array (PBGA).

A less expensive version, the 56302, will follow in 2Q96. The 302 exchanges the 301's PCI bus for a whopping 34K of on-chip RAM. The RAM is divided into 20K of program storage and 14K of of data memory, 4K of which may be converted to additional program memory. Because it has no PCI interface, the 302 fits into a 144-lead TQFP package.

Although many audio applications require 24 bits of internal precision, they do not necessarily need a 24-bit external data bus. Future derivatives of the 56300 family may use a 16-bit bus to reduce cost. The 301 can already operate in a 16-bit mode that effectively ignores the eight most-significant data bits.

The company is using a 0.5-micron three-layer-metal process for the first members of the 56300 family. As the die photo in Figure 1 shows, a relatively small proportion of the 56301 is actually devoted to the 56300 core.

Price & Availability

The first implementation of the 56300 core, the 56301, is currently in production at 66 MHz. The price in 100,000-unit quantities is $48. Pricing for the 80- and 100-MHz versions has not been released. For more information, contact Motorola (Austin, Texas) at 800.845.6686; fax 512.891.3877.

Motorola's Premium DSP

A 66-MHz 56301 is priced at $48 in 100,000-unit lots, which is significantly more expensive than most DSP processors. AT&T's DSP1627, for example, is priced at $49 in quantities of only 1,000. However, the 56301 carries significantly more peripheral logic and on-chip RAM, and delivers better performance. For the time being, at least, Motorola is charging a premium price for its premium part.

Motorola has staked out a clear lead at the high end of fixed-point DSP technology. Whether that move translates into a leading market position depends on the success of home theatre systems, videoconferencing support, and other high-end multimedia applications. The 56301 signals a bold start to an impressive product line. The company's challenge will be to find OEMs willing to pay for so much performance. ♦

Phil Lapsley is the editor of the Buyer's Guide to DSP Processors, *available through Berkeley Design Technology (Fremont, Calif.) at 510.791.9100.*

