Motorola Defines ColdFire Core Again

Three New Processors Establish New ColdFire Instruction Set

by Jim Turley

Motorola's original CF5102 has been joined by a trio of new ColdFire processors with substantially lower price tags, and one comes with moderate on-chip I/O. All three begin sampling over the next eight months. The new processors are touted as "real" examples of the ColdFire architecture, with reduced instruction sets and simplified fault models. In the process, the original 5102 has become something of an anomaly, neither wholly ColdFire nor entirely 68000.

The new 5202 and 5203 are conventional standalone microprocessors with small caches and moderate performance. The 5206 trades its cache for a memory controller and other peripheral functions. All three are welcome additions to a family that evidently has a long gestation period: the first ColdFire announcement was at the 1994 Microprocessor Forum, more than a year before these chips will even begin sampling.

68000 Instruction Set Gets Modified Again

Each of the three new chips has an identical core and, as Table 1 shows, similar features. The part numbering is significant. The 52xx chips have a different instruction set than the 5102 *(see **081405.PDF**)*. The smaller, simpler core in the new chips represents a more accurate example of the basic ColdFire concept of cost-reducing the 68K architecture. The 5102, in contrast, uses an "enriched" version of the ColdFire design—which is to say, the entire 68EC040 instruction set.

The first ColdFire design was based on the 68040 core and implemented every one of its instructions except those that deal with the FPU or MMU. The lower-cost 68EC040 version has no FPU or MMU, so for all practical purposes, the 5102 is a repackaged 68EC040 with smaller caches, a different bus interface, and a 42% lower price tag.

The code compatibility between the 680x0 CPUs and the 5102 made the latter chip attractive as a bridge for developers considering ColdFire as an alternative to upgrading along the historical 680x0 family line. The chip's lower cost allows it to be used in production, as HP has done with its LaserJet 5P and 5MP printers *(see **0903MSB.PDF**)*, while still using existing 680x0-family compilers. Apart from privileged system-level code, the 5102 will run 68EC040 binaries unmodified.

The same cannot be said of the new 52xx parts. They do not implement many familiar 680x0 instructions, such as BCD arithmetic, bit-string instructions, logical rotates, decrement-and-branch, integer division, and integer multiplication with 64-bit results. Four memory-indirect addressing modes have also been excised. Compiler writers and assembly-language programmers are encouraged to treat the 5200 series as a baseline for new ColdFire software development.

Application code written for the 52xx can be executed directly by the 5102, or by a 68020 or later-generation 680x0 processor. System-level code that accesses configuration registers or performs other low-level functions is generally not portable, even among ColdFire implementations.

	5102	5202	5203	5206
Max freq	25 MHz	33 MHz	33 MHz	33 MHz
MIPS*	19 MIPS	25 MIPS	24 MIPS	13 MIPS
I-cache	2K	2K	2K	512
D-cache	1K	unified	unified	512 SRAM
Address	32 bits	32 bits	32 bits	32 bits
Data	32 bits	32 bits	16 bits	32 bits
DRAM ctrl	No	No	No	Yes
Serial	None	None	None	2 ports
Parallel	None	None	None	12 bits
Timer	None	None	None	2
Process	0.6µ 3LM	0.65µ 3LM	0.65µ 3LM	0.65µ 3LM
Voltage	3.3 V	5 V	5 V	5 V
Package	PQFP-144	TQFP-100	TQFP-100	PQFP-160

Table 1. The three new ColdFire chips deliver performance similar to the original 5102. *based on Dhrystone 1.1 (Source: Motorola)

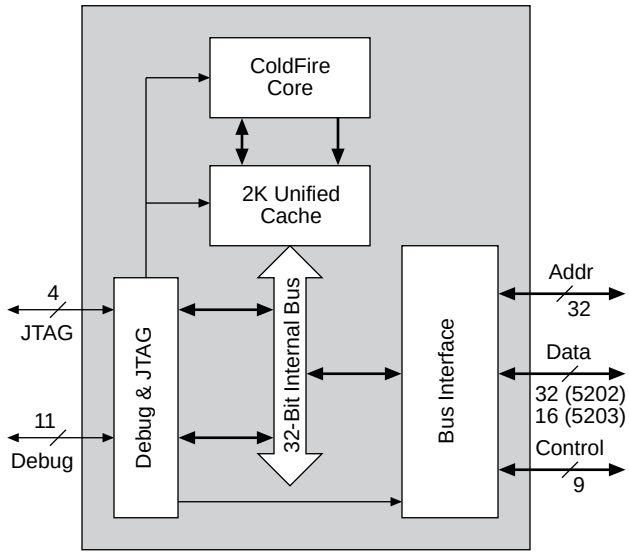

Figure 1. The 5202 and 5203 ColdFire chips are identical with the exception of the external data bus width.

5202 and 5203 Differ in Data Bus Width

As Figure 1 shows, the 5202 and 5203 are nearly identical, the only difference being the width of their external data buses. Both chips have the same core, 2K unified cache, and debug module. The multiplexed external address/data bus has 32 address lines and either 32 (in the case of the 5202) or 16 (for the 5203) data lines. The narrower data bus gives the 5203 somewhat lower performance on standard benchmarks but may be more appropriate for cost-sensitive applications that don't use 32-bit-wide memories.

Even though it has a narrower data bus, the 5203 has the same number of pins and the same package as the 5202, because data is multiplexed onto the 32-bit address bus. The two chips are, in fact, pin-compatible. To get some advantage from this situation, Motorola designed the 5203 to continue driving its low-order address lines while data is transferred on the upper half of the multiplexed bus. For cache-line fills, the least significant address bits automatically increment at every word address. These features make the 5203 a bit simpler for hardware designers to interface to standard logic than the 5202, which requires external latches and an address counter.

On simulated Dhrystone 1.1 runs, the 5202 produces 25 MIPS at 33 MHz; the 5203 is right behind, at 24 MIPS. The latter chip's half-sized data bus will make a bigger difference in many applications, but Dhrystone fits largely in the cache and is relatively immune to the reduced bandwidth. ColdFire's nominal 16-bit instruction word also helps keep the 5203 well stocked with opcodes across a 16-bit bus. This performance is within a few percent of the 5102's, confirming that the 68040's additions to the instruction set are not useful in Dhrystone execution.

5206 Adds DRAM Controller

The third part of Motorola's triple announcement is the 5206, an integrated microcontroller. Using the same core design as the other two devices, the 5206 adds a DRAM controller, eight chip selects, a timer, two UARTs, a Centronics-compatible parallel port, and an I²C serial interface, as Figure 2 shows.

Although the 5206 has a core identical to those in the 5202 and 5203, its performance plummets to 13 MIPS on Dhrystone simulations because it has only a 512-byte instruction cache and no data cache. Taking advantage of the chip's 512 bytes of on-chip data memory boosts the 5206's benchmark score to 17 MIPS.

All three chips are fabricated in a 0.65-micron three-layer-metal process—the same one used for many 68000-family processors. Unlike the 5102, the newer chips are 5-V–only devices. Motorola has said only that prices will be "less than $20."

Price & Availability

Motorola intends to begin sampling the MCF5202 and MCF5203 in 4Q95, with production in 2Q96. Final pricing has not been disclosed, but is expected to be around $20. The MCF5206 will begin sampling in 1Q96. For more information, contact Motorola (Austin, Texas) at 512.891.2917; fax 512.891.4568.

Roadmap Points to Faster Parts

Motorola is now beginning to reveal its plans for future ColdFire improvements. Moving to smaller geometries (0.5 micron and eventually 0.35 micron) *(see **0912MSB.PDF**)* enables the clock rate of existing designs to be dramatically increased. But in embedded applications, a 50- or 75-MHz bus is unworkable if not downright impossible. Thus, future ColdFire chips will have to run their external buses at some fraction of the pipeline frequency, as other vendors have done.

The company has shown that it can successfully merge different CPU cores in a single device: witness the PowerPC-based 821 and 860 *(see **091202.PDF**)*, the 68360, and the 68356 with its on-chip DSP unit. Future ColdFire implementations could also add DSP, communications, and floating-point units as needed. Particularly in the telecommunications and data-communications markets, Motorola has a rich and varied library of function units for application-specific peripherals. The current stable of ColdFire chips is just a start, and Motorola intends to extend this family, just as it has with its popular 68300 microprocessors. ♦

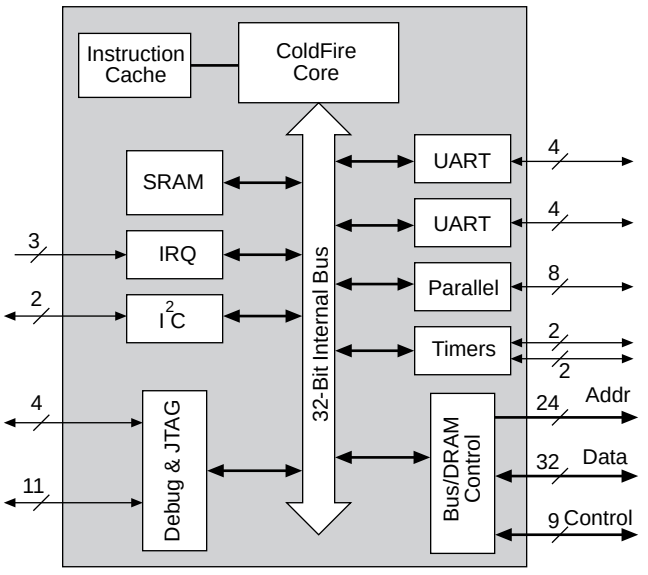

Figure 2. The 5206 is the first ColdFire component to have an integrated DRAM controller and other peripheral features.

