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National Pushes 486 into Embedded Market

Company's First x86 CPU, with On-Chip Peripherals, Sells for $25

by Linley Gwennap

For its latest run at the 32-bit embedded market, National Semiconductor has chosen the widespread x86 architecture, giving the company instant access to a wide range of embedded software and development tools. Taking advantage of its experience with PC peripheral chips, the company has combined a number of PC-compatible peripherals with its own 486-class CPU core. The result is a highly integrated system on a chip that sells for as little as $15, less than half the price of any other 486.

AMD and Intel aggressively pushed the 386 into the embedded market as it faded from the desktop. Although these companies are currently selling their desktop 486 chips to some embedded customers, National is ahead of the curve by producing a 486 designed specifically for embedded applications. By tuning its chip, the company can deliver low-end 486 performance at 386 prices. The NS486 does not, however, support DOS or other PC operating systems; National is aiming it at intelligent office and consumer devices.

Embedded x86 Market Is Large Target

National has had moderate success in the very low end of the embedded market with its 4-bit and 8-bit COP processors. These market segments currently have minimal growth, however, and the company has long eyed the fast-rising 32-bit embedded segment.

The 32000, which debuted in 1985, was National's first attempt in this area. Although it was originally positioned as a desktop processor, for lack of takers the 32000 quickly became an embedded device. The company released derivative chips for graphics products and had some success in X-terminals and printers. But the 32000 was eventually overrun by the i960 and other RISC chips; National continues to sell the 32000 family but does not recommend it for new designs.

More recently, the company deployed the Piranha processor core *(see **081502.PDF**)* for embedded applications. This RISC-like core comes in 16-bit and 32-bit versions. The two versions are not only incompatible with other existing instruction sets, they are incompatible with each other. These cores are available in custom parts for applications that don't require compatibility. Despite Piranha's tiny (as small as 3 mm^2) core, it delivers good performance: 16–21 Dhrystone MIPS.

National's 486 can't match the price/performance of Piranha, although it does turn in a respectable 12 Dhrystone MIPS at its initial speed of 25 MHz. The x86 architecture has attracted a large following in the embedded market, and National hopes to tap into this infrastructure. The existing software and tools base, as well as the ability to use a standard PC as a development platform, allows NS486 users to rapidly prototype applications and bring them to market. Thus, the chip is well suited for products in which time to market is critical, as long as the designer is willing to accept a higher per-unit cost.

National designed its 486 core entirely from scratch for the embedded market. The company licensed some technology from Integrated Information Technology's 486 project *(see **0809MSB.PDF**)*, but National says that it did not use any of IIT's logic or circuit designs in its chip. Instead, the company benefited from IIT's tools, particularly x86 compatibility tests. National hopes that its patent cross-license agreement with Intel and "clean-room" core design will avoid any legal issues with the x86 instruction set.

National's chip is not compatible with existing x86 processors at the hardware level; as a result, the number of hardware development tools for the NS486 is limited. Microtek plans to provide an in-circuit emulator (ICE) for the chip, and National will deliver evaluation boards.

Subset of 486 Functions

By developing its own 486 core, National was able to tune the CPU core specifically for embedded applications. For the most part, these changes eliminate 486DX features that are not used in most embedded applications, such as virtual memory, 8086 compatibility, and

floating-point support. These simplifications reduce both die size and power consumption.

National's chip operates only in protected mode, omitting both real mode and virtual-8086 mode. Once the chip has been booted and initialized in protected mode, many x86-based operating systems will run on the NS486. DOS, however, will not.

Without support for virtual memory, the NS486 needs no paging unit or TLB. The chip does have a segmentation unit and supports the standard x86 segmentation model. Effective addresses are translated into 32-bit linear addresses as in a standard 486, but the linear address is then used directly as the physical address without any further translation.

Like many embedded processors, the NS486 has no FPU. All floating-point coprocessor instructions are trapped, allowing software emulation for applications that require floating-point calculations but are not performance sensitive.

The company skimped on other features included in Intel's 486DX. The National design includes only 1K of instruction cache and no data cache rather than the 8K unified cache in Intel's part, another move to reduce the die size. The small instruction cache is adequate to speed the inner loops of many embedded applications and is particularly helpful in avoiding repeated accesses to slow external ROMs. The lack of data cache is alleviated by the on-chip DRAM controller, which can fetch data from main memory in as few as two cycles at the NS486's relatively slow CPU clock rate.

The NS486 is a full 32-bit core, but it implements a 16-bit data bus to memory and peripherals. Nearly all 486 processors intended for PCs have used a 32-bit bus to improve performance. For embedded systems, however, 16-bit buses are a common means of reducing package cost, footprint, power dissipation, and system costs.

Figure 1 shows the NS486 core, which contains 256,000 transistors. Intel's 486 integer core consumes roughly twice as many, indicating that National's simplifications provided significant savings. The savings are even greater considering that a full 486DX, including 8K of cache and an FPU, requires 1.2 million transistors. National would not reveal the die size of its new processor but said that, in the initial 0.65-micron three-layer-metal process, the core measures 29.6 mm^2, including the 1K cache. Intel's 486DX, not including pads, takes up 70 mm^2 in a 0.8-micron three-layer-metal process.

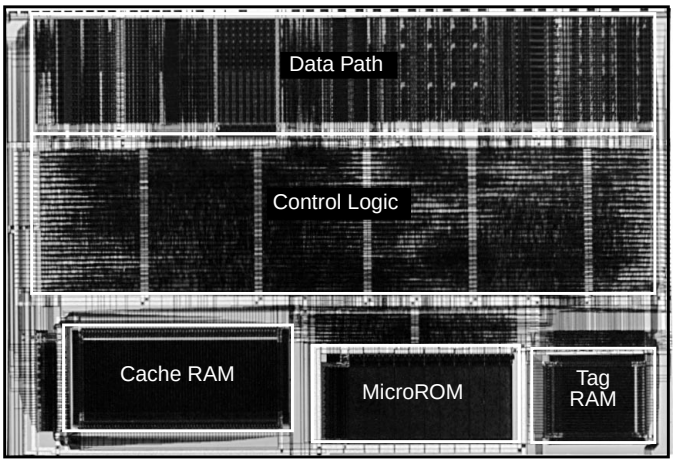

Figure 1. The NS486 is fabricated in a 0.65-micron, three-layer-metal CMOS process. The CPU core, shown here, measures 29.6 mm^2 and contains 256,000 transistors.

Trading Speed for Cost Savings

The National core implements a simple three-stage pipeline: fetch/decode, execute, writeback. The first stage of the pipeline is kept short by use of a prefetch buffer that is filled from the instruction cache by autonomous prefetch logic. The buffer has two entries that each hold eight bytes.

By combining all instruction execution into a single stage, National has created a critical timing path that reduces the clock speed: in a 0.65-micron process, the NS486 tops out at 33 MHz, whereas a standard 486 can achieve twice that speed in a less advanced 0.8-micron process. The shorter pipeline simplifies the control logic and reduces the need for bypassing while allowing the chip to match the cycle counts of a standard 486 on most instructions.

In short, National has wisely traded clock speed to get a smaller die. With a standard five-stage pipeline, the NS486 probably could reach 80–100 MHz in its 0.65-micron process, but this level of performance is not needed for National's target applications. Instead, these designs require the lowest possible cost, which National has attempted to meet by keeping the die small.

The company plans to address higher-performance applications by shrinking its new core to a 0.35-micron process in 1996. This shrink should boost the clock speed to 66 MHz or more while further reducing costs. Again, had National chosen a five-stage pipeline, the 0.35-micron version would have ticked along at 133 MHz or so, a speed few embedded designers want to cope with.

Some may argue that National's chip, with a tiny cache, 16-bit bus, and no FPU or TLB, is not really a 486. It is certainly not a 486DX-class processor and is not suited for PCs. For most embedded applications, however, the NS486 offers the necessary feature set while delivering performance far exceeding that of any 386 and comparable to a standard 486.

A Highly Integrated System

To the 486 core, National has added a wide range of peripherals, as Figure 2 shows. The low-cost NS486SXL includes a DRAM controller, DMA unit, two serial ports, an interrupt controller, and other PC-compatible system logic. Table 1 specifies the capabilities of

these peripherals, many of which were taken from National's popular PC "super I/O" chip. To this mix, the NS486SXF adds a PCMCIA controller, parallel port, and LCD controller.

Both chips initially use the same die, but National plans a separate design for the SXL in the future. The SXL keeps cost down by using a 132-pin PQFP, while the SXF requires a more expensive 160-pin package.

The DRAM controller drives all the control signals needed for common memory chips. Using fast-page-mode DRAM, the NS486 can fetch 16-bit data from memory in two cycles on a page hit (or three cycles for a new page); this capability allowed National to avoid an on-chip data cache. At 33 MHz, the two-cycle fetch requires expensive 50-ns DRAMs; at a more leisurely 25 MHz, 70-ns parts can be used. On burst accesses, the NS486 can achieve single-cycle throughput from memory.

Both chips include an "ISA-like" 16-bit bus for connecting to DRAM and external peripherals, including the PCMCIA device supported by the SXF. This bus can connect directly to most ISA peripheral chips, but some older 8-bit devices, as well as devices that use both CS16 signals, require extra glue logic. Nine programmable chip selects reduce the need for external address decoding.

With this peripheral mix, the $25 SXF is suitable for high-end office automation and communications devices that might have a small LCD display, a high-speed parallel port, or a PCMCIA card. The SXL version, which sells for just $15, is aimed at lower-cost devices that have restricted I/O demands.

National's power target for the 25-MHz version is 600 mW at 5 V, or just 260 mW at 3.3 V, making the chip attractive for portable systems. The NS486 does not support Intel's SMM but has its own power-management capabilities. The initial device does not support Geos or other existing PDA operating systems; National may target PDAs with a future 486 variant.

The NS486 was originally intended for Microsoft's At Work OS, but Microsoft has found few customers for this product and may discontinue it. National's chip also supports a number of common real-time operating systems, including pSOS+, QNX, VxWorks, and VRTX.

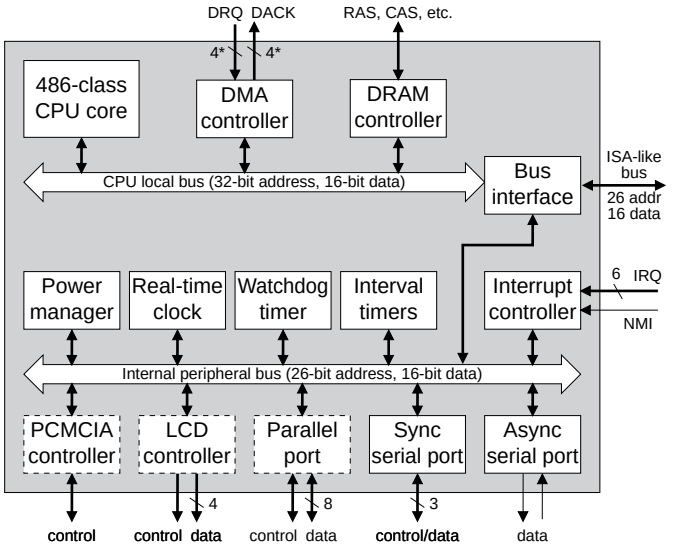

Figure 2. The NS486 combines a 486-class processor core with a 16-bit bus and on-chip peripherals. Dotted lines indicate modules included in the SXF version but not the SXL version. *2 in SXL

National Leapfrogs Embedded 386s

A fortunate confluence of events (see sidebar) leaves the NS486 practically alone in the embedded 486 market. Its real competition comes from 386 chips. Based on Dhrystone MIPS, these chips deliver about a third of National's performance, making the NS486 a winner for 386-based products that need more horsepower. With its integrated peripherals, the chip is a good upgrade for systems using Intel's 386EX or AMD's 386SC (Elan).

Many embedded designers, however, get by with static, low-power 386s from AMD or Intel that offer few, if any, on-chip peripherals. These chips sell for as little as $10, undercutting National's prices. Thus, potential customers must be captivated by either the performance or the peripheral set of National's chip.

One worthy competitor would be a 486-based version of AMD's 386SC. We believe AMD is developing such a device for HP *(see **0907MSB.PDF**)*, which it will probably build in a 0.35-micron process. AMD plans to sell this device as a standard product, but it is not expected to hit the market until late 1996, well after the

Peripheral	Capability
DRAM controller	Two banks up to 8M each; parity optional; supports page mode, CAS-before-RAS, self-refresh DRAMs
DMA controller	Four channels (SXF) or two channels (SXL); transfers 16 bits every two clock cycles
Interrupts	Two 8259-compatible controllers; 15 programmable interrupts; 6 external (plus NMI)
Interval timer	Three channels; 8254-compatible; CH2 can be a watchdog timer
Real-time clock	DS1287-compatible with 50 bytes of CMOS RAM and 3 maskable interrupt sources
Async serial port	NS16550-compatible PC standard UART with 16-byte FIFO; infrared support (Irda v1.0)
Sync serial port	Supports two-wire Access.bus or three-wire Microwire protocols
Parallel port	IEEE 1284–compatible 8-bit parallel port with host and slave ECP modes
PCMCIA port	Controls one PCMCIA 2.0 card; ExCA 1.5 and XIP capabilities; hot insertion requires external buffers
LCD controller	1 or 2 bits per pixel; resolutions up to 480 x 320; 60–90-Hz refresh rates
General I/O	Up to 29 bits if the above functions are not used

Table 1. The NS486 includes a variety of PC-compatible peripherals, many taken from National's "super I/O" chip.

An Opening in the 486 Market

While both Intel and AMD are major players in the embedded 386 market, neither has made a strong push with the 486. Intel recently moved responsibility for its 486SX, SX2, and DX parts to its embedded group, and the DX2 is likely to follow by the end of this year. The company has gained a few embedded design wins for these parts but to date has made no effort to redesign them for embedded applications, as it did with its 386 chips, instead using its stock desktop designs.

Indeed, Intel's embedded 486 efforts have been conducted rather quietly. The problem is a lack of trailing-edge fab capacity. By the end of this year, three of Intel's four 0.8-micron fabs will be converted to more advanced processes, and most of the remaining capacity will be consumed by Intel's booming chip-set business, leaving the embedded group with limited ability to service high-volume customers. Intel's more advanced process capacity is too expensive for embedded products and is also booked solid by high-profit Pentium chips; over time, some of this capacity should become available for embedded devices.

AMD's 486 business is currently focused on high-performance desktop chips. The company previously announced plans for a 486SE product for the embedded market but has now shelved this device in favor of a fully featured 486DE. This new product remains unannounced and is unlikely to reach the market before National's embedded 486.

Other 486 vendors include Cyrix, IBM, Texas Instruments, and SGS-Thomson, all of which are working from Cyrix's 486 core. Cyrix itself says it will stop shipping 486s by the end of this year, focusing its efforts on the 5x86 and M1; IBM is likely to follow a similar strategy. TI and SGS will probably service ongoing 486 demand but have no announced plans to redesign their chips for embedded applications.

NS486. In fact, National should have its own 0.35-micron version ready by then.

If x86 compatibility is not required, National's solution does not compare well with RISC-based processors. Chips such as the ARM710, SH7604, and V810 deliver more performance and lower power dissipation for about the same price as National's product. None of these chips, however, sells for less than National's $15 price, so for applications that need no more than the 12 MIPS delivered by the 25-MHz NS486, National is competitive.

Price & Availability

National plans to sample 5-V, 25-MHz versions of the NS486SXF this month, with volume production in 4Q95. Versions that support 3.3-V and 5-V operation at speeds up to 33 MHz, as well as the SXL version, are expected to sample in December and achieve volume production in 1Q96. In quantities of 10,000, the SXF will sell for $25 with the SXL priced at $15. For more information, contact National at 800.272.9959 x608 or send e-mail to *ns486@arador.nsc.com*.

Two-Pronged Approach Satisfies Needs

With its Piranha and NS486 lines, National covers both ends of the market spectrum. For high-volume applications that require strong performance at minimum cost, a custom part with a Piranha core is appropriate. For applications that require x86 compatibility, the NS486 offers the best price/performance among currently available 32-bit x86 processors.

One area this strategy does not address is low-volume designs. To gain flexibility, these designers typically use standalone processors with limited peripheral sets. National has no plans to offer the NS486 (or, for that matter, Piranha) as a standalone CPU, and it would have to offer a broader range of hardware development tools and support to gain lots of smaller embedded customers. Instead, the company seems happy to seek a relatively small number of high-volume design wins.

With the first products shipping by the end of this year, National will reach the embedded 486 market before any of the major x86 players, significantly increasing its profile in the microprocessor market. These products are well designed for their target applications. With its low price, the NS486 will appeal to 386 customers looking for an upgrade path and willing to use a real-time OS instead of DOS. ♦

