IBM Creates PowerPC Processors for AS/400

Two New CPUs Implement 64-Bit PowerPC with Extensions

by Linley Gwennap

Moving aggressively to convert its AS/400 line to RISC, IBM rolled out a line of minicomputers based on two new PowerPC processors. The CPUs, known as the A10 and A30, implement the full 64-bit PowerPC instruction set along with some extensions designed to speed AS/400 software; the company calls this extended instruction set PowerPC AS. These extensions could appear in mainstream PowerPC chips in the future.

The new systems replace nearly the entire AS/400 line, which has an installed base of more than 300,000 systems. The new models start as low as $9,000 for the A10-based Model 400; pricing for the A30 systems was not announced but could start around $200,000. Products using the A10 will ship in volume in 4Q95, with the higher-end systems shipping in 1Q96.

Previous AS/400 systems used a CISC architecture called IMPI. IBM has been planning for an instruction-set transition for years; the AS/400 is unusual in compiling software into an intermediate form as well as a binary form. The company has developed tools to convert this intermediate code into PowerPC instructions, so applications will execute in native mode on the new systems. IBM has no plans for an IMPI emulator and does not believe that its customers will need such a tool.

Multichip A30 for High Performance

The new A30 is a truly impressive processor, executing up to four instructions per cycle with a minimum cycle time of just 6.5 ns (154 MHz). As Figure 1 shows, it consists of seven chips in a multichip module. This design appears similar to that of the Power2 processor *(see **071301.PDF**)*, but the two IBM processors were designed by separate teams and share no circuitry.

The CPU chip contains an 8K instruction cache, while the four cache chips implement a 256K data cache that also acts as a level-two instruction cache. Due to the MCM package, the data cache can be accessed in a single cycle, even at 154 MHz. The MCM also allows a wide, 256-bit bus from the data cache to the CPU. In addition, the CPU can fetch 256 bits (8 instructions) per cycle from its internal instruction cache, generating a total peak cache bandwidth of 9.8 Gbytes/s. The miss penalty for the instruction cache is just two cycles.

Because large commercial applications overwhelm most branch-prediction techniques, the A30 eschews prediction; with its awesome bandwidth, it can fetch from both the target and the sequential addresses until the branch is resolved. This feature, coupled with the relatively short six-stage pipeline, virtually eliminates branch penalties. If the instruction setting the condition code is issued ahead of the branch, there is no branch penalty. There is a single-cycle penalty if the condition-code instruction is paired with the branch and the branch is taken.

The A30 achieves its high clock speed despite using an antiquated 0.72-micron BiCMOS process; the processor would probably exceed 200 MHz in IBM's 0.5-micron process. In the current process, the CPU and FPU chips measure 209 mm^2 and the cache chips are 238 mm^2. The design supports symmetric multiprocessing with up to four A30 processors.

It is difficult to compare the performance of this processor to that of other PowerPC chips because the company has not ported AIX and the SPEC benchmarks to the AS/400. IBM estimates that the A30 will approximately match a PowerPC 620 on a clock-for-clock basis; since the 620 currently tops out at 133 MHz, the A30 should outperform that chip.

A10 Reaches Low Price Points

The A10 is a single-chip design aimed at a lower price/performance point. To reduce upfront design cost, IBM chose an ASIC methodology, resulting in a big, slow chip. The processor consumes 213 mm^2 (larger than a 604) in IBM's 0.65-micron CMOS process and reaches a peak speed of just 77 MHz. IBM estimates the clock-for-clock performance of the three-way superscalar A10 at

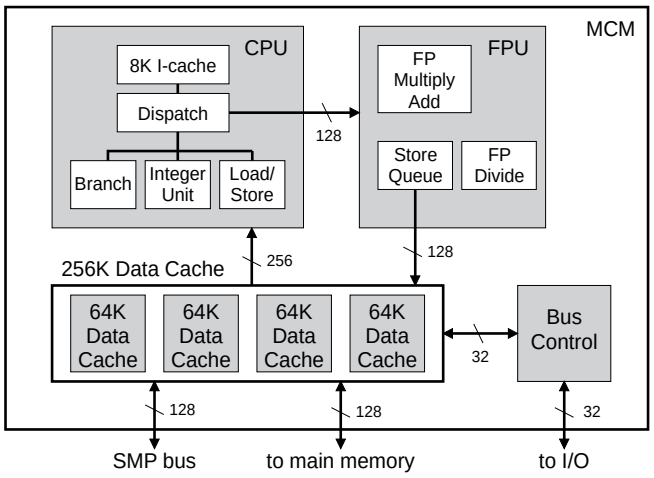

Figure 1. The A30 processor consists of seven chips in a single package. The MCM package enables wide buses that deliver high bandwidth among the CPU, cache, and main memory.

Price & Availability

The A10 and A30 processors are not available for sale as components. For more information on the PowerPC-based AS/400 systems, contact your local IBM sales office, dial IBM's fax service at 800.IBM.4FAX, or check the World Wide Web at *http://www.as400.ibm.com*.

about that of a 604, putting the core performance of the 77-MHz chip about on par with that of a 100-MHz 601. The A10 is further hampered by having just 4K of instruction cache and 8K of data cache.

IBM could not use one of the PowerPC 60x chips to meet this price point because the AS/400 requires a 64-bit architecture, and the 620 is the only existing 64-bit PowerPC chip. Both the A10 and A30 also implement a special addressing model, which includes new instructions and an additional protection flag for each cache line, to support AS/400 programs; existing PowerPC chips lack this feature.

Along with the new addressing model, the PowerPC AS extensions include double- and quad-word loads and stores, a vectored call instruction, and instructions to assist decimal arithmetic. These instructions, similar to existing PA-RISC instructions, have minimal impact on die size and clock rate; even the extra cache bits would add less than 1% to the total die area of most processors.

IBM could incorporate all the AS extensions into its midrange and high-end PowerPC chips, leveraging a single design across its various product lines and providing manufacturing economies of scale. Alternatively, it could take future 64-bit cores and add these extensions, although this would introduce a technology lag between the AS/400 and RS/6000 lines, and it would require building two different sets of processors. IBM is evaluating ideas like these to avoid developing completely new chips for future PowerPC-based AS/400 systems.

Ultimately, this strategy should reduce IBM's processor development costs by leveraging PowerPC across all its products from PCs to large servers. IBM has no current plans to move its mainframes to PowerPC, but massively parallel PowerPC systems are beginning to take on mainframe applications. Like HP and Digital before it, IBM is moving to unify the bulk of its product line around a single RISC architecture. ♦

