Intel Plugs i960 into PC Servers

Integrated i960RP Has Dual PCI Buses, APIC, and DRAM Controller

by James L. Turley

Reversing a time-honored trend of resisting system-level integration, Intel has produced a feature-rich version of its i960 embedded processor. The new 960RP is tailored for servers, with a number of features for accelerating busy I/O subsystems, especially in systems based on Intel's P6. The chip complements the P6 and furthers Intel's goal of increasing the proportion of silicon with Intel logos in each PC.

The 960RP's functions, performance, and aggressive pricing should make it attractive to Compaq, Dell, and other makers of PC-based application servers. The processor can also work alone as a single-chip I/O processor in networking, telecommunications, bridge, and router applications.

The new microprocessor integrates the existing 960JF core and caches with two independent PCI bus interfaces, a conventional 960-style bus, a DRAM controller, three DMA channels, and extensive interrupt-management logic. In a server, the 960RP could manage network and storage controllers on one PCI bus, buffer the data using its integral DRAM controller, and forward data packets to the host over the other PCI bus. The chip, which is not expected to ship until 4Q95, has a target price of less than $50 in OEM quantities, only one-third higher than the 960JF on which it is based.

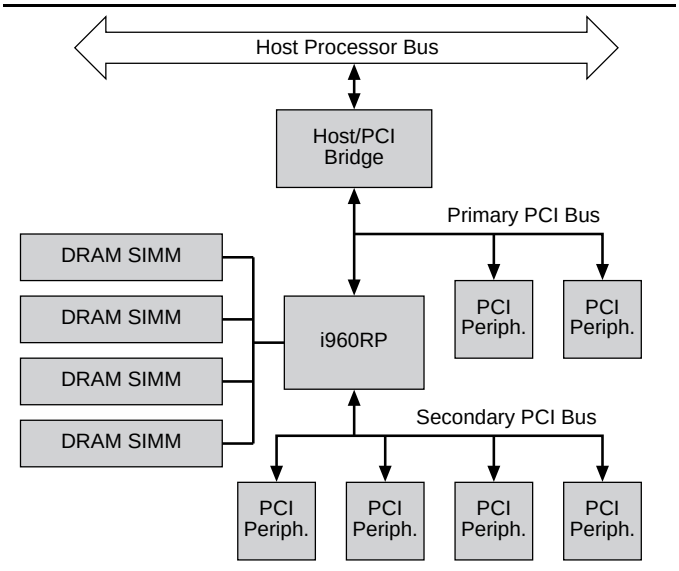

Figure 1. When used in a PCI-based server system, the 960RP appears as another PCI expansion device. All peripheral devices on the 960RP's secondary bus are logically separated from the main PCI bus, under control of the 960RP processor.

PCI Bus Fits with Server Architecture

The RP's unusual dual-PCI feature is also its most vital in the context of PC servers. The purpose of the dual buses is twofold: to give the 960RP a more standard interface to I/O chips and to separate a host system's PCI backbone into intelligent and nonintelligent portions.

In a typical system, the primary PCI bus connects to the host processor, typically through a local-bus bridge. The system's peripheral controllers then reside on the 960RP's secondary PCI bus, as Figure 1 shows. In effect, the chip splits the PCI bus in two, inserting itself between the host processor and peripherals. From the point of view of the host CPU, the 960RP is another PCI peripheral chip.

The 960RP delivers the most benefit when allowed to handle the setup, initialization, and management of the downstream peripherals, offloading these tasks from the host CPU. The host's role may then be as simple as issuing generic read or write requests to the 960RP, leaving the details to device drivers in the 960RP's local memory.

In a multithreaded operating system, the OS could maintain a linked list or queue of I/O requests. As the 960RP processes requests, it returns the requested data to shared memory until the queue is empty again.

The host initiates I/O requests by writing to the 960RP's messaging unit, a set of registers that appear in the PCI address space. One of the two primary DMA channels then transfers a command block from system memory into local DRAM. Peripherals on the secondary PCI bus then carry out the requested transaction, including transferring network or storage packets directly into the 960's local DRAM. A final DMA transfer moves the complete packet into system memory, and the 960RP signals completion of the transaction by updating a command-complete queue and interrupting the host CPU.

Address Translation Eases Routing

Two address-translation units—one on each PCI port—allow the part to act as a three-way crossbar. Bus masters on either PCI bus can access resources on the other. Resources on the 960RP itself, such as the local memory, I^2C interface, and I/O APIC, can be accessed from either PCI bus for setup and configuration.

The chip also includes a PCI bridge. The window of addresses that pass through to the secondary PCI bus is programmable; the inverse range of addresses is automatically passed from the secondary to the primary PCI

bus, avoiding unwieldy aliasing problems. Bridge traffic from one PCI bus to the other does not impact the local bus, so processing can continue.

Downstream PCI devices can be declared private to the 960RP, hiding them from the host CPU. During PCI configuration, the host polls the bus, identifies each device, and allocates address space for it. The 960RP can intervene in this process, effectively hiding selected peripherals from the host CPU. This could be useful to guarantee exclusive access to particular peripheral devices on the secondary bus.

Private peer-to-peer transactions are possible between two PCI chips on the secondary bus. This allows two intelligent controllers to exchange data without impacting traffic on the primary PCI or the local bus.

Integration Is New to 960 Family

The 960RP includes several features, shown in Figure 2, designed to make it self-sufficient. The memory controller supports up to 256M of DRAM or SRAM in interleaved or noninterleaved configurations. The chip drives RAS, CAS, and WE as well as 12 multiplexed address lines. Data flows over the chip's 960-style local bus. Signal timing is compatible with fast-page-mode, EDO (extended data out), or burst EDO DRAMs.

Although the 960RP's native 32-bit multiplexed system bus is completely functional, few designers will use it for anything other than a data path between the CPU and local memory. Apart from Intel's own 82961KD printer coprocessor, few 960-compatible peripheral chips exist, while the number of PCI-compatible peripherals is growing. Retaining the local bus on the 960RP allows users to leverage existing 960-based logic or keep local resources (like a boot ROM) off either PCI bus.

Both PCI interfaces support the specified limit of 10 loads apiece, with add-in cards counting as two loads. The chip's arbiter has enough pins for six PCI masters on the secondary bus. For a fully loaded secondary bus, users must develop their own PCI arbiter. The internal arbiter implements a prioritized round-robin arbitration scheme, allocating PCI bus mastership equally among chips of the same priority.

The advanced priority interrupt controller (APIC), so dear to the Pentium and P6 designs, makes its first appearance outside the x86 world in the 960RP. By including an I/O APIC to complement the APIC in Pentium and the P6, Intel is making it as easy as possible to include the 960RP in Intel-based multiprocessor systems.

A New Direction for the 960

The development of the 960RP is evidence of Intel's new direction for its embedded microprocessor division, which only recently changed its written charter to better serve applications "in and around" Intel-based PCs. The 960's historic success in laser printers and network routers and bridges could be interpreted as furthering that goal. But the 960 has always been a "generic" processor with no particular application-specific features. Hewlett-Packard, for one, likes it that way, preferring to develop its own application-specific circuitry and relying on Intel for CPUs. Now Intel has stepped over that line, moving squarely into the data-communication and PC-server markets.

Thus far, Digital's 21066 and TI's failed Rio Grande have been the only microprocessors with a PCI interface—ironic, considering that Intel developed the bus. In the PC server market, PCI makes obvious sense, and other embedded, industrial users are eyeing PCI and PMC (PCI mezzanine cards) for expansion as well. The 960RP's combination of features may help get it into those applications.

With the first step already taken, more derivatives of the 960Rx probably aren't far behind. A printer-control processor could leverage Intel's experience with the 82961KD. As with its strategy for PCs, Intel wants a larger portion of every system to be Intel silicon. The 960RP is another step in that direction. ♦

Price & Availability

First samples of the 33-MHz 80960RP will be available in 4Q95, with volume production starting in 2Q96. The chip is packaged in a 352-lead plastic ball-grid array (PBGA). The volume price has been set at $48.85 in 10,000-unit quantities. For more information, contact Intel (Chandler, Ariz.) at 800.626.7256.

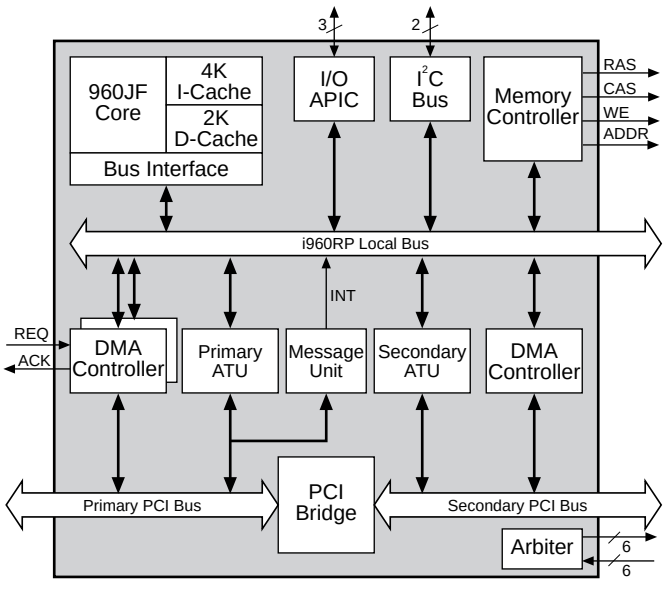

Figure 2. Intel's 960RP has two independent PCI buses with a bridge between them. The dual address-translation units (ATUs) map addresses from PCI to the 960RP local bus. The messaging unit allows PCI bus masters to interrupt the 960 core.

