# Intel Releases Pentium Errata List

## Most Known Bugs Fixed in Latest "C2" Stepping

**by Linley Gwennap**

For the first time in its history, Intel has publicly disclosed the list of bugs and other problems in one of its flagship processors. The newly released document shows that early versions of Pentium, in production throughout 1993 and 1994, had dozens of minor bugs. Most of these flaws are invisible to end users, but a few, including the infamous FDIV problem, are not. The most recent versions, which are just now entering production, fix most of the known problems, resulting in fairly clean chips.

Intel has decided to release its errata list to the public in the wake of criticism for failing to disclose the FDIV problem in a timely fashion. The errata document describes known bugs and their workarounds; it has historically been circulated to system makers (OEMs) and key software vendors (ISVs) under nondisclosure agreements. The company plans to update the errata list monthly, disclosing bugs to the public about 30 days after their descriptions are distributed to OEMs and ISVs.

Intel's disclosure is unusual: MIPS Technologies is the only other microprocessor vendor that provides such documentation. This move will ensure that small OEMs and ISVs will have access to the errata list, which has not always been true in the past. Although most system buyers will find its dense prose unenlightening, the document allows analysts and savvy users to better evaluate the risk of purchasing a processor. Another motivation *(see **0903ED.PDF**)* is to get the buying public accustomed to the idea that all microprocessors have bugs.

At this time, the new policy applies only to Pentium. Intel expects to follow the same policy for the forthcoming P6 processor but would not reveal the errata lists for older devices such as the 486. Sources indicate that, even today, the 486 carries a number of bugs that have not been corrected, and Intel is not interested in fixing them at this late stage in the processor's life. With tens of millions of 486s in the field, one can assume that these bugs are insignificant to end users.

### Steppings Denoted by Letter/Number Pair

The errata document provides insight into the production process of a typical Intel microprocessor (and processors in general). During the development of a chip, the design goes through several iterations, or steppings. The first silicon fabricated is the A-step or A0 stepping, in Intel's terminology.

As bugs are found, the design must be corrected and retested. The designers are often able to fix bugs by changing only one or two metal layers; since the metal layers provide the interconnects, these changes "rewire" the design. By not changing the circuit layers, the possibility of introducing a new error is reduced and, in some cases, the production process can be accelerated. For metal-only changes, Intel increments the numeric portion of the stepping name, from A0 to A1, for example.

If there is a particularly severe problem, or an accumulation of minor problems, the design goes through a revision in which all mask layers are changed. Intel indicates these major revisions by incrementing the letter, from A1 to B0, for example.

Once a part reaches volume production, the vendor often continues to make mask changes. Some may be to correct bugs that are discovered after the chip is released. Other changes may improve yield. As with the development process, some of these changes may affect only metal layers, while others may cause the entire design to be revamped.

### Pentium Production History

Intel's documents show that both the initial P5 Pentium and the P54C Pentium achieved volume production on the B-step, indicating that each chip required only one complete mask change to achieve volume production.

The 0.8-micron P5 has gone through three production steppings: B1, C1, and D1. The C1 stepping fixed seven bugs, none of which affect end users. The D1 stepping, which entered production early this year, corrects 10 more bugs, including the FDIV flaw, and includes some changes to improve frequency yield. The current stepping does not, however, fix the FIST bugs described below.

Intel is currently shipping only D1 versions of the 60- and 66-MHz Pentium, although some system makers may still be selling PCs with C1 parts, depending on their inventory levels. Intel has no plans for additional P5 steppings that would correct the outstanding bugs.

The 0.5-micron P54C version has a more checkered history. Based on the P5 design, the chip adds support for multiprocessor systems via new APIC logic *(see **080301.PDF**)*. The P54C is available in a new TCP package *(see **081503.PDF**)*, which also added to the errata list. In less than a year since its release, the P54C has gone through B1, B3, B5, and C2 production steppings. The gaps indicate steppings (e.g., B2) that did not reach production. Intel says that it often plans intermediate nonproduction steppings to test some designs.

The B3 stepping corrected six minor bugs, including two that occur only in the TCP version. The B5 stepping

 

| No. | Status | Errata (Description) |
|---|---|---|
| 1 | Fixed in C2 | Branch trace messages during lock cycles. |
| 2 | Fixed in C2 | Breakpoint or single-step may be missed for one instruction following STI. |
| 3 | Fixed in C2 | I/O restart does not function during single stepping or data-breakpoint exceptions. |
| 4 | Fixed in C2 | NMI or INIT in SMM with I/O restart during single-step mode. |
| 5 | Fixed in C2 | SMI# and FLUSH# during shutdown. |
| 6 | Fixed in C2 | No shutdown after IERR#. |
| 7 | Fixed in C2 | FLUSH# with a breakpoint pending causes false DR6 values. |
| 8 | Fixed in B3 | Processor core many not serialize on bus idle. |
| 9 | Fixed in C2 | SMIACT# premature assertion during replacement. |
| 10 | No fix planned | STPCLK# deassertion not recognized for five clocks after BRDY# returned. |
| 11 | Fixed in C2 | Future Pentium OverDrive processor FERR# contention in two socket systems. |
| 12 | Fixed in B3 | Code cache lines are not invalidated if snooped during Autohalt or Stop Grant states. |
| 13 | Fixed in B3 | STPCLK# assertion during the execution of the HALT instruction hangs system. |
| 14 | No fix planned | NMI or INIT during HALT within an SMM may cause large amount of bus activity. |
| 15 | No fix planned | RUNBIST not operational when run through boundary-scan circuitry. |
| 16 | No fix planned | FRC mode miscompare due to uninitialized register. |
| 17 | No fix planned | STPCLK# restrictions during EWBE#. |
| 18 | Fixed in C2 | Multiple allocations into Branch Target Buffer. |
| 19 | Fixed in C2 | 100-MHz REP MOVS speed path. |
| 20 | Fixed in C2 | Overflow undetected on some numbers on FIST. |
| 21 | Fixed in C2 | Six operands result in unexpected FIST operation. |
| 22 | Fixed in B3 | Snoop with tablewalk violation may not invalidate snooped line. |
| 23 | Fixed in B5 | Slight precision loss for floating-point divides on specific operand pairs. |
| 1DP | Fixed in C2 | Problem with external snooping while two cycles are pending on the bus. |
| 2DP | Fixed in C2 | STPCLK# assertion and the Stop Grant bus cycle. |
| 3DP | Fixed in C2 | External snoops with AHOLD asserted may cause processor to hang. |
| 4DP | Fixed in C2 | Address parity check not supported in dual-processor mode. |
| 5DP | Fixed in B5 | Inconsistent cache state may result from interprocessor pipelined READ into a WRITE. |
| 6DP | Fixed in C2 | Processors hang during zero-wait-state pipelined bus cycles. |
| 7DP | Fixed in C2 | Bus lock-up problem in a specific dual-processor-mode sequence. |
| 1AP | Fixed in C2 | Remote read message shows valid status after a checksum error. |
| 2AP | Fixed in C2 | Chance of clearing an unread error in the Error Register. |
| 3AP | Fixed in C2 | Writes to Error Register clear register. |
| 4AP | Fixed in C2 | Three interrupts of the same priority cause lost local interrupt. |
| 5AP | Fixed in C2 | APIC bus synchronization lost due to CS error and RR message. |
| 6AP | Fixed in C2 | HOLD during a READ from local APIC register may cause incorrect PCHK#. |
| 7AP | Fixed in C2 | HOLD during an outstanding interprocessor pipelined APIC cycle hangs processor. |
| 8AP | Fixed in C2 | PICCLK reflection may cause an APIC checksum error. |
| 9AP | Fix planned | Spurious interrupt in APIC through-local mode. |
| 10AP | Fixed in C2 | Potential for lost interrupts while using APIC in through-local mode. |
| 1TCP | Fixed in B3 | CPU may not reset correctly due to floating FRCMC# pin. |
| 2TCP | Fixed in B3 | BRDY# does not have buffer selection capability. |
| **No.** | **Status** | **Specification Changes (Description)** |
| 1 | New in B5 | New pin definition (CPUTYP). |
| 2 | Documented | Timing addition for BRDYC# when driven synchronous to RESET. |
| 3 | Documented | PICCLK specification changes. |
| 4 | Documented | PCHK# has weak drive, not open drain, in dual-processor mode. |
| 5 | New in C2 | BRDY# and FRCMC# pullups added. |
| 6 | Documented | Mixing steppings in dual-processor mode. |
| 7 | Documented | MD/VR/VRE specifications. |
| 8 | Documented | CPUTYP pulldown default. |
| 9 | Documented | CLK toggle during Vcc ramp. |
| 10 | New in C2 | Lock-step APIC operation mode. |
| 11 | New in C2 | Package change to replace metal lid with ceramic lid. |
| 1TCP | B-step only | AC timing changes for TCP mobile package. |

Table 1. All published errata and specification changes for Intel's P54C Pentium processor, as of February 1995. DP indicates dual-processor mode only, AP indicates APIC (multiprocessor systems only), and TCP indicates items that affect only TCP parts. (Source: Intel)

 

fixed only the FDIV bug and one multiprocessor bug. Apparently, one reason that Intel took so long to put the FDIV fix into production is that it hoped to go directly to the C-step but was waiting to accumulate a number of changes for that stepping.

The C2 stepping provides a major housecleaning for the P54C. It removes a total of 28 bugs that are present in earlier steppings, including 15 bugs that affect only multiprocessor systems. Some of these bugs are discussed in detail below. According to the document, there are six known bugs in the C2 stepping, only one of which Intel plans to fix in the future; the others have relatively simple workarounds. Intel is currently producing a mix of B5 and C2 parts and intends to move entirely to C2 production by the end of this quarter.

The C2 stepping also reduces the P54C die area by about 10% using an optical shrink, making the new die area 148 $mm^2$. After building millions of chips in its 0.5-micron process, Intel used its experience to trim the minimum feature sizes by 5%. Instead of completely redoing the chip layout to take advantage of the new rules, the company simply reduced the full-size mask set much as a copy machine would reduce a document.

The smaller die eases the P54C manufacturing cost to $105, according to the MDR Cost Model, 10% less than the previous cost. It also slightly increases the capacity of Intel's fabs and, more important, improves the percentage of parts that operate at 100 MHz. This improvement allowed Intel to slash the price of the 100-MHz Pentium by 28% last month *(see **0902MSB.PDF**)*.

## Classifying Pentium Errata

Intel's errata document purports to list all known deviations between the Pentium processors and the publicly available data books. The document does not cover errata that apply to the secret Appendix H features of Pentium; these errata (of which there are a few) are available only under NDA to OEMs and ISVs.

The deviations are divided into four categories. *Errata* are what most people would call bugs. Most of the errata have been or will be fixed, although some have been documented as features. *Specification changes* include some bugs that are being documented instead of fixed, as well as other minor changes to the original documentation. *Specification clarifications* describe situations that are not clearly documented in the Pentium manuals. Finally, *documentation changes* correct typos or other errors in the original documentation.

Table 1 lists all errata and specification changes in the P54C Pentium. In addition to this list, which contains 42 errata and 10 specification changes, there are 8 specification clarifications and 5 documentation changes. As the status column shows, most of these bugs have been corrected in later steppings of the chip. The P5 errata list (not shown) is significantly shorter, as that chip is not impacted by the DP, AP, and TCP problems described in the table. The P5 list consists of 21 errata, 4 changes, 16 clarifications, and 2 documentation changes.

| Processor Stepping | CPU_ID Family | Model | Step | Lot Numbers (on package) |
|---|---|---|---|---|
| P5 B1 | 5 | 1 | 3 | SX753–SX754 |
| P5 C1 | 5 | 1 | 5 | SX835–SX837 |
| P5 D1 | 5 | 1 | 7 | SX948–SX974, SX976- |
| P54C B1 | 5 | 2 | 1 | SX874–SX910 |
| P54C B3 | 5 | 2 | 2 | SX921–SX951, SX960 |
| P54C B5 | 5 | 2 | 4 | SX957–SX959, SX962, SX975 |
| P54C C2 | 5 | 2 | 5 | SX963–SX970, SX976- |

Table 2. The stepping of a Pentium processor can be determined via software, using the CPU_ID instruction, or by examining the lot number on the package, as described in the text.

One way to determine the stepping level of a particular Pentium chip is to use the CPU_ID instruction. After executing this instruction, bits [3:0] of the EAX register contain the stepping level, as Table 2 shows. A software utility is available from Intel to display this value.

The stepping can also be determined by reading the markings on the top of the package. The first set of numbers identifies the part: "A80501-60" indicates a 60-MHz P5, for example, while "A80502-100" designates a 100-MHz P54C. The next set of numbers can be mapped to the stepping, as Table 2 shows. (The table applies only to production parts; sample units are marked differently.) The table includes lot numbers that are assigned as of February 1995; Intel may assign new lot numbers in the future. Numbers greater than 975 should indicate the current (or future) steppings.

## Potential End-User Impacts in B-Step

Intel has declined to classify the bugs in any way, feeling that its categorization could be seen as biased and judgmental. This attitude, which hopefully will change in the future, leaves users with little guidance in interpreting the lengthy errata list. Our analysis shows that six bugs (18–23) could potentially affect end users by causing software to execute improperly in very unusual situations. All six have been fixed in the C2 stepping of the P54C, but two remain even in the latest P5 stepping.

Number 18 involves an error in the branch target buffer (BTB). A long sequence of events, including a specific pattern of taken/not-taken branches, can result in the same branch being allocated into multiple entries in the BTB. Additional events may cause these entries to contain conflicting branch predictions. If this branch is then accessed, a drive fight in the circuitry causes incorrect information to be written into the instruction cache.

Because this random data is likely to contain a parity error, accessing it will assert the IERR# signal more than 90% of the time. This error signal usually forces an application error or a system reset. Even if IERR# is not signalled, the application will probably exhibit some

 

## For More Information

To receive a copy of the Pentium errata list, contact the Intel Literature Center at 800.548.4725 or P.O. Box 7641, Mt. Prospect, IL 60056. Ask for the *Pentium Processor Specification Update*. For technical information on any of these issues, call Intel's support hot line at 800.628.8686.

clearly unusual behavior caused by executing random instructions, indicating the error to the user.

Although this sequence of events is convoluted, it happens to lurk within Windows versions 3.10 and 3.11. This bug affects all B steppings of the P54C but not the P5, which uses a slightly different circuit design.

Number 19 affects only early shipments of 100-MHz Pentium chips. The bug causes an additional data item to be transferred when a REP MOVS instruction executes with the source and destination within the same cache line, and the bug is triggered by a cache snoop. Because of the low incidence of cache snoops in uniprocessor systems, this bug has been observed only in MP systems. The bug is caused by a critical speed path and thus is dependent on voltage, temperature, and process variation. Intel has been screening out this problem for months, and the C2 stepping fixes the speed path.

The FIST (convert FP to integer and store) instruction is the source of errata 20 and 21. This infrequently used instruction does not detect an overflow condition on certain large FP numbers, instead returning a value of zero. The affected numbers are 65,535.5±0.5 in 16-bit mode and 4,294,967,295.5±0.5 in 32-bit mode, a small fraction of the total input space. Note that these values are approximately twice as large as the maximum acceptable value in these modes.

In addition, six specific operands are improperly rounded in certain modes. These operands are ±0.0625, ±0.125, and ±0.1875. Positive values are incorrectly rounded to 0.0 in "up" mode, while the negative values are incorrectly rounded to 0.0 in "down" mode.

One workaround is to use the FRNDINT (round FP to integer) instruction before FIST. Intel says that it found only a few end-user applications that use FIST, and these always execute FRNDINT first. Another workaround is to use the "chop" rounding mode. Not coincidentally, both ANSI-C and FORTRAN default to the chop mode. (Intel used these languages to develop test programs.)

The exposure to end users is small, but it is possible that a little-known application could trigger the problem and receive an incorrect result without any indication of an error. This invisibility contributed to the panic over the FDIV problem. The FIST bug is present in all versions of the P5, including the new D-step, and in all versions of the P54C prior to the C2 stepping.

Under certain conditions, a cache snoop with invalidation may fail to invalidate the indicated entry in the instruction cache, as described in erratum 22. Because this snoop could be caused only by a write to an address in the instruction cache, it affects only self-modifying code. The sequence of events that causes this error has never been observed in a real system; this bug was discovered by examining schematics. It is present only in the B1 stepping of the P54C as well as in the B1 and C1 steppings of the P5.

Number 23 documents the FDIV problem, which has been extensively discussed *(see **081702.PDF**)*. It is fixed in the B5 and D1 steppings of the P54C and the P5, respectively.

### Many Multiprocessor Problems Fixed

Multiprocessor systems are extremely complex to debug. Bugs are often caused when a particular sequence or combination of events occurs on the system bus. Synchronizing the instruction streams on two or more processors well enough to reproduce a problem is tricky, making it difficult to isolate and resolve these problems. Running enough test cycles to find these bugs in simulation is nearly impossible.

After the initial release of the P54C, Intel discovered a number of problems in dual-processor and multiprocessor configurations. All these bugs (except number 19, as noted above) are seen only by the system designer, that is, the system hardware must provide a workaround to prevent these bugs from affecting proper program execution. These workarounds, however, sometimes have a significant performance impact.

Several of these bugs require that bus pipelining be disabled. Pipelining allows the processor to assert the address for the next transaction during the previous transaction. Intel estimates that disabling pipelining will reduce system performance by about 8%. Number 7DP prevents B-step Pentiums from operating with zero wait states, reducing performance by 2–4%. These limitations are removed in systems using C-step parts.

Some of these problems arise only with third-party chip sets. Intel extensively tested the P54C using its own Neptune chip set. Many third-party chip sets, however, were not available when the P54C was first released. These chips sets exposed bugs in the processor that could not be repaired until the C-step, a pattern that is likely to repeat with future processors.

Number 9AP is the single pending flaw in the C2 stepping that Intel plans to fix in a future version. This bug causes spurious interrupts to be reported when using the APIC in 8259-compatibility mode. One workaround is to use the I/O APIC in the system logic for compatibility; another is to rewrite the software.

These bugs make it difficult to mix processors of different steppings in an MP system. A workaround

 

required by an earlier stepping may not work with a newer chip, or it may inhibit performance. Most current MP systems must be upgraded by the vendor to ensure a proper match. The next crop of MP systems will ship with C-step processors, allowing end users to easily upgrade their systems by adding a new CPU.

## Little to Worry About in C2 Stepping

So far, the C2 stepping looks to be a clean part. The errata list contains only six bugs, all of which can be avoided by careful system design. Only one of these bugs is considered serious enough to correct in a future stepping. The D1 stepping of the P5 Pentium is not in quite as good shape, given the unrepaired FIST problems. Intel expects to phase out the P5 for new designs over the next few months, but current customers are left in the lurch.

Keep in mind that Intel lists only known bugs with defined workarounds. At any given time, Intel is evaluating a number of reported bugs, most of which turn out to be elsewhere in the system. Pentium may contain bugs known to Intel that are not yet publicly released due to the company's 30-day disclosure process. In addition, the chip probably has undiscovered bugs that will arise in the future when the chip is used with new software, new chip sets, or in new configurations.

Intel's willingness to make its errata lists available on an ongoing basis will help end users assess the impact of these future flaws. The P54C errata list appears daunting; it is longer than the bug list for the R4400 and probably those of other RISC parts, although we still await the release of competitors' errata. Intel's processors are used with a far greater range of software and system logic than, say, a SPARC processor, so it is reasonable that its chips would have more errata. End users should be concerned with the magnitude, not the number, of errata and with how the vendor handles them. ♦

 