Hitachi SH-3 Hits 100 MIPS

New Chip Keeps Most Features, Increases Clock Rate to 100 MHz

by James L. Turley

From the depths of obscurity, Hitachi's SH7604 became the world's best-selling RISC microprocessor in just a year, thanks to Sega. Now the company is trumping its own high card with a faster third generation of this little-known processor family. The new SH7708 promises to deliver 100 Dhrystone MIPS while reaching a new low in power consumption and die size. Although the first parts won't be available until August, the SH-3 line should give 1995's upcoming embedded chips some stiff competition for handheld applications and big-ticket consumer electronics items.

Hitachi rates the new chip a whopping 300% faster than the previous top of the line, the SH7604, placing it well ahead of embedded PowerPC, 29K, and i960 chips, and within shouting distance of the R4200 and Pentium.

Faster Clock Buys Big Performance Gain

The functional differences between the SH7708 and the previous-generation SH7604 *(see **080203.PDF**)* are limited primarily to the selection of on-chip functional units, as Table 1 shows. Where the SH7064 has a separate integer divide unit and two-channel DMA controller, the SH7708 drops in an MMU and a larger cache. (A sister chip, the SH7702, has a 2K cache.) The lack of a divide unit means that the SH7708 cannot process other instructions in parallel with division, but the latency is one cycle per bit in either case. Unlike the SH-2 core, the SH-3 has no advantages over its predecessor; there are no new instructions, nor did the existing ones get any faster.

	SH7708	SH7604	960HT	602
MAC Unit	32-bit	32-bit	no	no
Divide Unit	no	yes	yes	no
FPU	no	no	no	yes
MMU	yes	no	no	no
Transistors	800K	450K	2300K	1000K
Cache (I/D)	8K	4K	16K/8K	4K/4K
32/32 Divide	37 cycles	37 cycles	39 cycles	37 cycles
32 ∞ 32 Multiply	3 cycles	4 cycles	5 cycles	5 cycles
Interrupts	8	8	8	3
Serial Ports	1	1	no	no
Counter/Timers	3	1	2	no
DMA Controller	no	2 channel	no	no
Clock Rate (3.3V)	100 MHz	20 MHz	75 MHz	66 MHz
Clock Rate (2.5V)	40 MHz	n/a	n/a	n/a
Dhrystone (3.3V)	100 MIPS	20 MIPS	125 MIPS	65 MIPS*
Dhrystone (2.5V)	40 MIPS	n/a	n/a	n/a
Power (3.3V)	700 mW	500 mW	4500 mW	1200 mW
IC Process	0.5 µ, 3M	0.8 µ, 2M	0.6 µ, 4M	0.65 µ, 4M
Die Size	44 mm^2	56 mm^2	100 mm^2	50 mm^2
Availability	1Q96	Now	2Q95	2H95
Est. Mfg. Cost	$11*	$14*	$50*	$14*
List Price (10,000)	$49*	$25*	$158	$45*

Table 1. A comparison of the SH7708 design with the current 7604 shows that the newer chip differs mainly in cache size and on-chip peripherals. (Source: vendors except *MDR estimates)

Most significantly, the maximum clock rate has almost quadrupled, from 28.5 MHz to an even 100 MHz. The SH7604's relatively dowdy 0.8-micron process and early-generation layout prevent it from running much beyond its current limit. By skipping the intermediate 0.65-micron process and going straight to 0.5-micron, the SH7708 opens a big performance gap between the two chips. The first two SH-3 chips to be sampled, a 60-MHz SH7708 and a 45-MHz SH7702, should fill that gap.

The SH7708 has a unified 8K cache, which may seem a bit restrictive for a relatively high performance microprocessor, but its fixed-length 16-bit instructions yield an effective increase in the amount of code that can be cached compared with 32-bit RISC chips. The cache is four-way set-associative, alleviating some of the mapping conflicts that might arise in a unified cache. Organized into 16-byte lines, the cache is virtually indexed and physically tagged, but no snooping is provided to keep it coherent.

Stores normally write through the cache; it may be switched to write-back mode for systems that do not share portions of memory with another bus master. A one-word write buffer allows the processor to retire store operations without tying up the whole chip during external write cycles.

First MMU Opens Doors to New Software

The SH7708 and SH7702 are the first SH chips to have an MMU. This marks a bold departure for Hitachi, and a calculated move into the PDA and set-top box market, where memory management and protection are required. The company has indicated it is encouraging (i.e., funding) ports of various embedded and PDA operating systems for this reason.

The address-translation scheme looks very similar to that used in embedded MIPS processors, such as IDT's R3051 family. Two privilege levels divide the logical address map into user space and supervisor space. The user can access only the lower 2G of memory; supervisor code can access the entire 4G range. The user model is unchanged from the SH7604.

As in MIPS chips, the first 2G is mapped straight across, aliasing the user's physical memory. The next two 512M segments also map down into low memory, the difference being that the first segment is cachable, while the other always forces a miss. The remaining space is divided in half: 512M is cachable, while the last 512M is reserved for I/O control, peripheral registers, and architectural extensions.

The four-way set-associative TLB holds 128 entries. Each logical address maps into one of 32 lines in the TLB. The TLB can optionally factor a 5-bit task ID into its hashing algorithm, forcing different tasks to map to different TLB lines, reducing thrashing among tasks.

The chip does not perform hardware table-walks; TLB misses must be handled in software. Also, the first attempt to write to an unwritten physical page causes a fault, allowing the operating system to enforce its own form of page protection.

The chip has only 26 address pins, as Figure 1 shows; its address range is extended via the seven chip-select outputs for a 448M physical address space. Although the chip has a normal 32-bit data bus, provisions have been made for embedded systems that put more emphasis on control than on processing. Through a programmable option, data bits 16–23 may be converted to a bidirectional 8-bit parallel port; meanwhile, the rest of the chip has to make do with a 16-bit data bus while data bits 24–31 lie unused.

Flexible Clocking Options Save Power

The ability to control a processor's clock rate, and hence its power consumption, is becoming a common feature with new embedded chips. The SH-3 chips follow this trend, with several options that allow the programmer to balance the performance requirements of the application against the demands of power dissipation.

Starting from a fixed crystal input, the SH7708 can operate the CPU core at 1×, 2×, or 4× the base frequency; the multiplier may even be changed on the fly. A 25-MHz crystal yields the maximum 100-MHz core frequency. The on-chip peripherals, conversely, can run at 1×, 1/2, or 1/4 the speed of the input clock. The CPU and peripheral clocks are independent; a 100-MHz core with peripherals running at 6.25 MHz is possible.

Unused peripheral functions (counter/timers, serial port) may be shut down when not in use. A SLEEP instruction stops all core activity while peripherals keep operating; standby mode stops all internal and external activity while reducing power consumption to just a few microamps of leakage current.

One interesting trick Hitachi played to keep current draw low came from the company's SRAM development organization. In the cache, word-line sense amps are energized only for the one set that hits while the other three stay switched off. At 100 MHz, the amps' warm-up time is not a factor in the cache's performance. The sense amps themselves are much more sensitive than normal, responding to just a 60-mV differential. Apart from saving power, this design allows the word lines to be asserted and negated more quickly than with a full-voltage design.

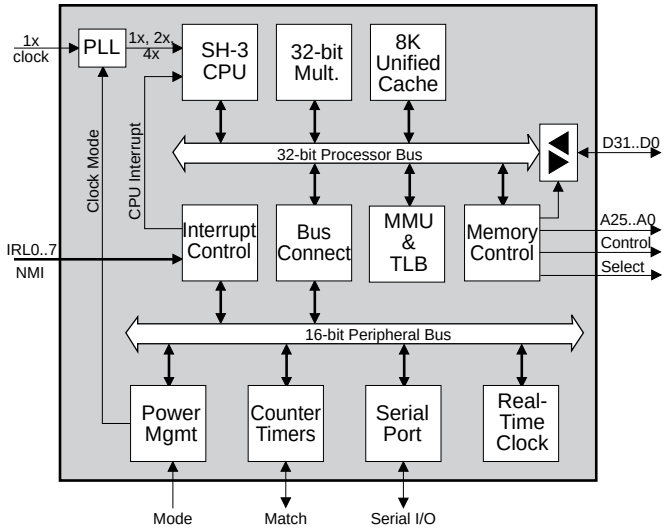

Figure 1. Hitachi's SH-3 architecture uses the same execution units as the SH7604 but sacrifices the independent divide unit for larger caches and an MMU with a 128-entry TLB.

Low Power Sets Hitachi Chip Apart

The chips are rated for 2.5–3.3 volts, although maximum clock rate suffers at lower voltage. A nominal 100-MHz part is limited to 40 MHz at 2.5 V, while a 60-MHz SH7708 peaks out at 25 MHz at 2.5 V.

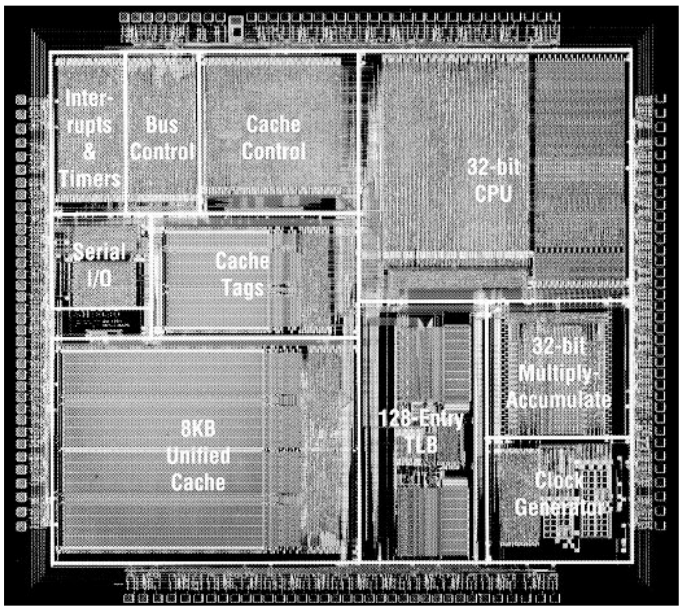

Figure 2. The SH7708 devotes nearly half of its die to the unified cache and associated control logic. Less than 20% of the 44-mm^2 die is taken up by the CPU core.

Price & Availability

Volume production of the 60-MHz SH7708 and 45-MHz SH7702 is expected to begin in August. The 100-MHz SH7708 will follow in 1Q96. Final pricing has not yet been disclosed. For more information, contact Hitachi America (Brisbane, Calif.) at 415.589.8300.

All this speed comes at a price: the SH7708 typically dissipates 700 mW at 100 MHz, far higher than, say, an ARM710 (which also has an 8K cache, MMU, and TLB) at 105 mW or IBM's 403GA (with its DRAM controller, timers, and serial port), at 200 mW. At first glance, the SH7708 seems power-hungry compared with chips with similar features.

That might be a hindrance if there were any comparable chips that could match the SH7708's performance. Like Digital's Alpha processor, the attraction is not that the chip runs "efficiently" at high speed but that it runs at all. For embedded applications that urgently need 100 Dhrystone MIPS performance, the alternatives are few. The 68060 and 960HT are two embedded processors playing in the SH7708's performance ballpark, but they each dissipate 3–5 watts. An chip that can deliver 100 MIPS for less than one watt is a good deal, integrated peripherals or not.

With its 8K cache, the SH7708 measures 6.6 mm on a side in Hitachi's 0.5-micron three-layer-metal process. That size places it on par with the 403GA, which is built in a similar process. Less than 20% of the die is devoted to the SH7708 CPU core; the majority is consumed by the cache, cache tags, and cache control logic, as Figure 2 shows. When they become available, both the SH7708 and the SH7702 will use the same 144-lead PQFP as the SH7604, although the SH-3 chips will not be pin-compatible with the older part.

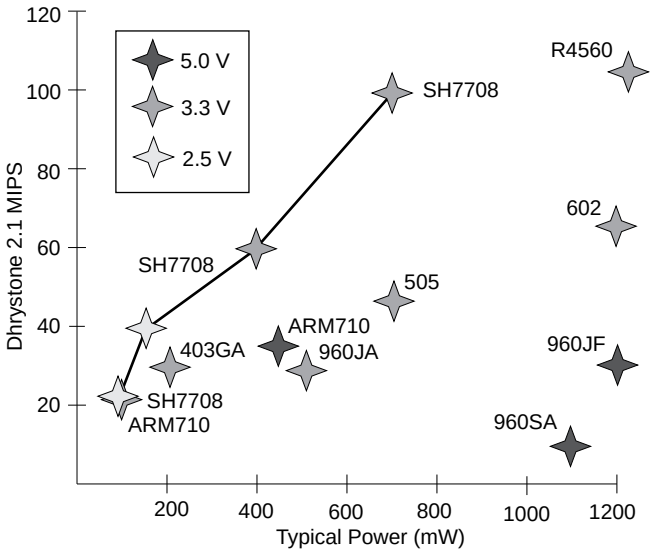

Figure 3. A comparison of power consumption for the SH7708 and other embedded processors shows that the Hitachi chip is particularly efficient at low voltages.

Hitachi is setting a target price of about $0.50 per MIPS, placing the 100-MHz SH7708 at $50. At about $30 for the 60-MHz version, the SH7708 is again equivalent to a 25-MHz 403GA, but the PowerPC chip delivers about two-thirds the performance.

On a MIPS-per-dollar scale, the SH7708 has everyone beat. Its target price is well under that of the 68060 or 960HT, at $300 and $150 apiece, and less than even IDT's $64 R4650. Except for the 68060, most other processors can't match the code-density advantages of Hitachi's fixed 16-bit instruction word, either.

A more worthy competitor might be found in Somerset's newest PowerPC 602 *(see **090203.PDF**)*. It is similar to the SH7708 in power dissipation, die size, manufacturing cost, and cache size. Integer performance for the initial 66-MHz 602 is similar to that of the 60-MHz SH7708, right down to their 37-clock, stepped 32-bit divide functions. An expected 80-MHz 602 will compete with the fastest SH7708, and the 602 throws an FPU into the bargain.

An 80-MHz R4650 *(see **081504.PDF**)* delivers comparable integer performance to the 100-MHz SH-3 but at a higher price and nearly twice the power (see Figure 3). Both the PowerPC and MIPS chips enjoy a considerable advantage in development tools and a much clearer growth path to higher performance numbers, both in integer and floating-point execution.

Breakthrough Chip for Hitachi?

Hitachi is well aware of its "stealth marketing" reputation for selling embedded microprocessors and is working to be considered more seriously as a top-tier processor vendor. Certainly the company has made a good start with its successful SH-2 product; if the SH-3 chips can garner another high-volume design, Hitachi will be on its way to becoming a processor powerhouse.

By adding an MMU, the company is clearly hoping to inject the SH-3 into set-top and PDA designs. Although the parts' technical merits will make them attractive alternatives to forthcoming ARM, PowerPC, and MIPS chips, it is not clear which PDA makers will want to adopt another architecture. Magic Cap and Newton, the two predominant PDA operating systems, are both being ported to new architectures. But Apple, Sony, and Motorola are unlikely to support another new hardware standard.

The SH product line is hobbled by lack of software and support tools and, more important, by a general lack of customer interest in the architecture. If Hitachi can paint itself as a reliable, full-service supplier of top-notch embedded microprocessors, the SH architecture may yet be rescued from obscurity. ♦

