Motorola Announces PowerPC System Logic

Spurs System Vendors with Design Kit, HAL Code for Windows NT

by Linley Gwennap

Aiming to simplify the design of PowerPC systems, Motorola and its partners have fired off a flurry of announcements. The most significant is that Motorola will market a system-logic chip, the MPC105, that will provide cache control, memory control, and a PCI interface for any PowerPC 60x processor. Although this chip is the second PowerPC system-logic design to be announced, it is the first with such a high degree of integration. Motorola expects to begin shipments by the end of this year.

The company also announced an evaluation system, known as Big Bend, that uses the ’105 chip in a PowerPC motherboard. Reply Corp. (San Jose, Calif.) will manufacture and sell Big Bend systems. A reference design similar to Big Bend will be available through Motorola and Cadence Design (San Jose, Calif.). Motorola also said that its previously announced development tools for Windows NT applications *(see **0808MSB.PDF**)* will be available for Microsoft’s “Daytona” release, the next version of NT, which is expected to ship imminently.

Eagle: One Chip Does It All

The ’105, code-named Eagle, delivers a significant improvement in integration over IBM’s system-logic chip set, the 82650 *(see **071601.PDF**)*. The IBM product includes two chips for memory and PCI interfaces plus an optional third ASIC to control the secondary cache; the ’105 includes all these functions in a single chip. Figure 1 shows a block diagram of a system based on the Motorola chip. The cache and PCI interfaces are entirely glueless, while the memory subsystem requires a few buffers, depending on loading.

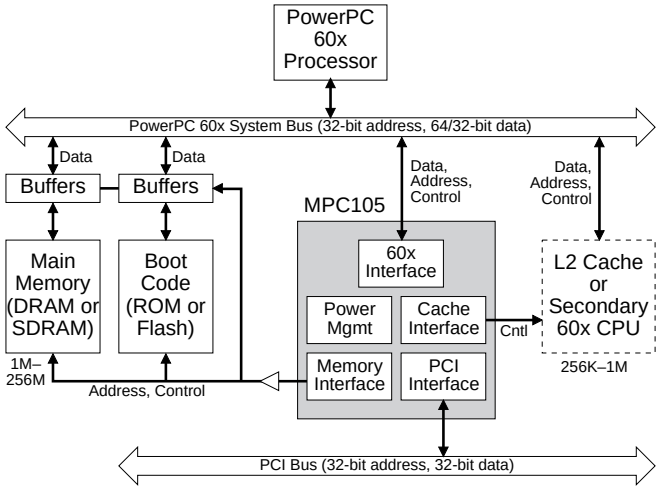

Figure 1. A typical PowerPC system using Motorola’s MPC105 requires little glue logic for cache, memory, and PCI interfaces.

The ’105 supports the PowerPC 601, 603, and 604 processors, all of which use a similar 64-bit system bus. Like the 603, the ’105 can operate with a 32-bit subset of this bus in very low cost systems. The system-logic chip allows system bus speeds up to 66 MHz. The CPU itself can then operate at a ratio of the system bus clock (typically 1:1, 3:2, or 2:1). The ’105 supports both burst and pipelined transactions on the system bus.

The external cache can be built with either standard SRAM or synchronous SRAM. With 9-ns synchronous parts, the cache will return data in three cycles for the first word (3-1-1-1 access rate) at 66 MHz. The cache can be 256K, 512K, or 1M in size, write-back or write-through, in a direct-mapped configuration. Cache tags must be implemented externally. The ’105 maintains consistency between the processor’s caches, the external cache, and the main memory.

The chip also allows for a limited multiprocessor configuration in which the external cache is replaced by a CPU chip. This concept supports the Prep “upgrade socket” that can hold either an external cache or an upgrade processor *(see **071704.PDF**)*. In the two-processor configuration, the ’105 maintains consistency between all caches and main memory.

The memory interface can control both the main memory subsystem—either standard or synchronous DRAM—and a boot ROM. Main memory size can be up to 1G using 16-Mbit parts; 1- and 4-Mbit chips are also supported. The Motorola chip supports a variety of DRAM widths and speeds and allows up to eight separate memory banks. Memory may be protected using byte parity but not ECC. With 60-ns DRAMs, the critical word is returned to the CPU in eight system bus cycles at 66 MHz (8-3-3-3 access rate).

The ’105 begins the main-memory access at the same time as the secondary cache access and aborts the DRAM read on a cache hit; this technique assures that the data is returned as quickly as possible on an external cache miss.

The boot code can be implemented with standard ROM or flash memory, to which the ’105 allows write access as well as reads. There are several options for locating the boot code, giving the system designer some flexibility. The boot ROMs can sit on the system bus, filling the entire 64- or 32-bit data bus, or they can sit on the 32-bit PCI bus or even the 8-bit ISA bus. There is also an option to put an 8-bit ROM on the system bus; in this case,

Price and Availability

Motorola expects to sample the MPC105 in 4Q94, with production in the same quarter. The company has not announced pricing for this part. For more information, contact your local Motorola sales office or call 800.845.6686 or 512.343.8940; fax 512.343.9509.

the ’105 accumulates ROM data in an internal buffer and then places the data on the system bus at the full width.

Because of a limited number of address signals, the maximum ROM size is 16M with a 64-bit data path or 2M with an 8-bit data path. When flash memory is used, one of the address signals is used as a write enable, halving the amount of boot memory that can be used.

Flexible System Interface

The PCI bus operates at the same or one half of the system-bus frequency, between 20 and 33 MHz. The ’105 supports more extensive buffering between the PCI bus, memory, and CPU than IBM’s chip set, reducing CPU stalls. With both the system bus and PCI bus operating at top speed, a single read from the CPU will typically complete in 12 cycles. The PCI interface will convert between big- and little-endian data if needed.

The Motorola chip incorporates a range of power-management modes similar to those in the PowerPC processors. Operating at 3.3 V, the chip draws about 1.0 W (typical) with all functions enabled and less than 100 mW in suspend mode.

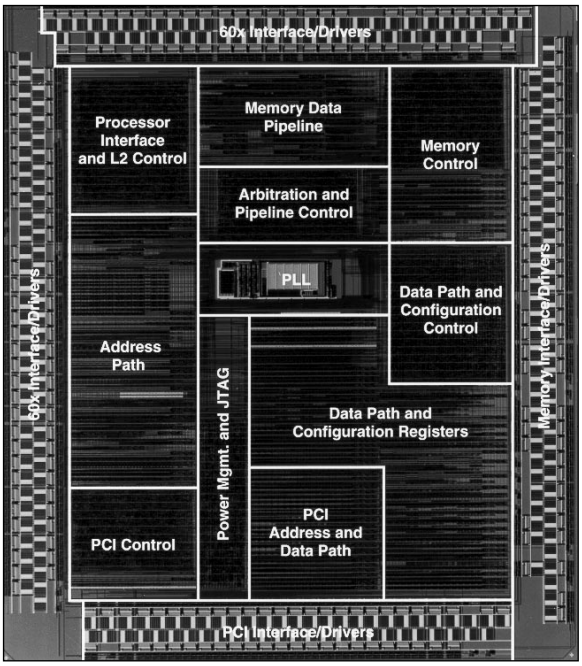

Figure 2. Die photo of the MPC105, which measures 6.7 × 5.8 mm and uses about 300,000 transistors in 0.65-micron CMOS.

The ’105 is built in the same 0.65-micron (drawn), four-layer-metal CMOS process as the 603 and 604. Figure 2 shows the die, which measures just 39 mm^2 . It is packaged in a 304-pin ceramic BGA. The MDR Cost Model *(see **071004.PDF**)* estimates the production cost of the ’105 to be about $25, with more than half of the cost in the package. Motorola hopes to move to a plastic BGA in the future to reduce package cost.

The die photo shows that the pads are arranged in two rows. Motorola is using a variant of IBM’s flip-chip (C4) bonding *(see **071304.PDF**)* instead of wire bonding. With traditional wire bonding, the ’105 die would have been much larger, as the pads would have been restricted to a single row around the outer edge of the die. This is Motorola’s first production part using flip-chip; if successful, the company may use this technique in its PowerPC processors as well.

Motorola plans to sample the ’105 in 4Q94, with production by the end of the year. The company has not yet announced pricing but says that the price will be competitive with that of IBM’s $65 chip set. Given the low cost of the single-chip design, this goal should be achievable.

Reference Systems Available

Motorola and its partners are providing a number of products to ease the design task of potential PowerPC system vendors. Motorola’s Big Bend evaluation system contains a motherboard, in a baby-AT form factor, that provides a complete Prep-compliant system based on either the PowerPC 603 or 604 processor and the ’105 system-logic chip. The board also uses the UMC 8886 PCI-ISA bridge, National’s Super I/O controller, and NCR’s SCSI controller.

The board comes with slots for two cache-memory cards and four DRAM SIMMs, as well as three PCI and three ISA slots. A 4-Mbit flash ROM stores the boot code. Using the National PC87323, it provides all common PC peripherals. The board also includes a 160-pin logic-analyzer port, connected to the system bus, for debugging purposes. A variety of graphics adapters can be added using a PCI slot.

The Big Bend standard system configuration includes an 80-MHz 603 processor, 1M of external cache, 32M of DRAM, and a 500M SCSI hard drive. The system also comes with two floppy drives, a CD-ROM drive, an Ethernet card, and an accelerated graphics board with 4M of VRAM. The system includes the necessary firmware and HAL (Windows NT hardware abstraction layer) code and has NT preinstalled on the hard drive.

Motorola is not selling these systems but will loan them to qualified hardware and software vendors developing for PowerPC. The systems are manufactured under license by Reply, which will sell Big Bend motherboards and systems. Reply has the right to develop derivative products, which it will likely do, as the Big Bend

design needs to be modified for high-volume production. (In particular, the logic-analyzer port should be removed to save cost.) Reply has not announced pricing for any PowerPC products.

For $50, Motorola will provide a manufacturing kit that includes schematics, board layout, Gerber file, and other information needed to build the Big Bend motherboard. No licensing fees are needed for this design information. The kit does not, however, include the source code to either the boot code or the HAL; this software can be obtained from Motorola for a "reasonable" licensing fee, or the vendor could choose to develop this code itself.

Cadence will sell a version of the design kit formatted for the company's EDA tool set. This package includes simulation, thermal, and analog models of key components as well as manufacturing information for the board. Cadence plans to deliver its design kits beginning in 4Q94 and has not yet announced a price.

Which Way from Here?

The blitz of announcements demonstrates Motorola's commitment to Windows NT on PowerPC. Although all Prep-compliant products are also compatible with IBM's OS/2 for PowerPC and AIX operating systems, Motorola's unstated belief seems to be that neither of these products will have much success outside of IBM, although Motorola will continue to support these platforms while letting IBM carry the promotion. Many system vendors also take a dim view of IBM's in-house operating systems but are sticking with the Prep platform to hedge their bets.

Motorola's backing of NT, however, simply adds to the software confusion surrounding PowerPC. While hardware vendors hedge, ISVs are faced with some hard choices: develop applications for the Power Macintosh, currently the only volume PowerPC platform; develop for OS/2 on PowerPC and bet on IBM to succeed; or go for NT and rely a multitude of small hardware vendors. Only the largest ISVs can afford to target two or more of these platforms; most will stick with just x86.

One advantage of NT is that software vendors can leverage NT development on other platforms, such as Pentium, in creating code for PowerPC. This code must still be recompiled, tested, and supported on PowerPC systems, however, so the vendor must see a significant market for such a product. So far, no major system vendors are strongly endorsing NT on PowerPC, and Motorola's recent announcements seem unlikely to change this fact. The design kits and other products make it easier for smaller companies to jump onto PowerPC, and perhaps enough of them, combined with second-tier players like Canon, can counter the weight of Apple on one side and IBM on the other.

This conflict could be resolved if Apple chooses to license the Macintosh operating system, as it is beginning to show signs of doing (see sidebar). Many PowerPC system vendors would rather sell Macintosh-compatible systems than Windows NT boxes, taking advantage of Apple's growing installed base of PowerPC systems. This could leave NT-on-PowerPC as a niche product on the desktop, although it would still be attractive for servers.

On the other hand, if Apple continues to hold its hardware and software close to the vest, ISV confusion will continue. Motorola has put together a strong case for Windows NT on PowerPC, but the big PC vendors will probably sit on the fence and see whether NT or OS/2 does well. Ultimately, Microsoft will move NT into the mainstream *(see **081001.PDF**)*, but without Apple's help, PowerPC may have to wait much longer before getting on track. ♦

Apple Could Play Key Role

While Motorola throws its weight behind Windows NT, it is keeping an eye on the possibility that Apple will license other vendors to build Power Macintosh clones. Apple has been talking about doing so for several months, so far with little to show for it. The latest rumors are that the company will announce several licensees at Comdex in November but will fall short of making System 7, its Macintosh OS, available on a broad basis. Potential licensees include vendors that could increase Macintosh's worldwide presence—such as Vobis (Germany) and Olivetti (Italy)—and current partners IBM and Motorola.

Such a targeted program will do little to increase Macintosh's overall market share. If Apple announces a broader licensing program, however, it could greatly increase the number of Macintosh (and PowerPC) systems shipped. One possibility is that Motorola will get the right to build Macintosh systems for small vendors.

Motorola would be pleased with any program that boosts overall PowerPC sales. The company notes that its '105 chip set includes some features to support System 7 memory mapping, although additional hardware would be required for Apple-specific peripherals, such as LocalTalk and ADB. Apple itself will probably use its own chip sets, but the '105 or a derivative could eventually find its way into Macintosh clones.

One fly in the ointment is that Apple and IBM have still been unable to agree on a way to merge the Prep platform with the Macintosh. In other words, Prep-compliant systems will not run System 7. It would be possible, however, to run Windows NT on a Power Macintosh by writing the appropriate HAL code.

Thus, if Apple does launch a broad licensing program, Macintosh hardware could become the defacto standard for PowerPC, knocking Prep out of the picture, except at IBM. Widespread availability of System 7 would allow ISVs to target their PowerPC applications at a single high-volume platform, solving the babel they face today. PowerPC, and Motorola, would thrive.

