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DSP Cores Bring New Levels of Integration

Core-based ASICs and Licensable Cores Create New Options

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One of the most interesting and important factors emerging in the DSP (digital signal processor) industry is the widespread use of DSP cores. Most simply stated, a DSP core is a DSP intended for use as a building block in creating a chip, as opposed to being packaged by itself as an off-the-shelf component. DSP cores, like other kinds of processor cores, have long been used internally by semiconductor vendors to help create multiple products based on a common processor architecture. Recently, however, DSP cores have begun to be used in some fundamentally different ways.

First, some DSP vendors (such as Texas Instruments and SGS-Thomson) are increasingly offering their volume customers the opportunity to design ASICs combining a standard DSP core with the customer's own logic, extra memory, and other elements. Second, specialty design houses (including DSP Group and Clarkspur) are beginning to offer DSP core designs under license to a wide range of semiconductor vendors, which may then use them to create their own standard parts or to offer DSP-based ASICs to their customers.

These trends mirror similar developments over the past couple of years in the general-purpose CPU and microcontroller markets, where semiconductor vendors like Motorola *(see **0807MSB.PDF**)* and LSI Logic will combine their processor cores with custom logic. LSI recently announced a major design win with Sony *(see **080902.PDF**)* based on its CoreWare program. HDL Systems *(see **071506.PDF**)*, like DSP Group, will license its MIPS core for customers to add to their own chip designs.

Core-based design is becoming increasingly important among volume users of DSPs, since it offers a combination of the best features of programmable processors and custom hardware. DSP-based ASIC users get the established support base of a standard processor—including development tools, software libraries, and programming expertise—along with the integration, power consumption, and performance advantages of custom hardware. The increased integration offered by this approach is essential for a growing set of DSP applications, such as PCMCIA modems and digital cellular telephones, that place a premium on physical size and power consumption. At the same time, the design of DSP-based ASICs requires new approaches from system designers and design tools (see sidebar below).

TI First to Combine Gate Array, DSP

Texas Instruments, long a major merchant supplier of standard DSPs, has combined its strengths in both DSPs and ASICs to take a leading role in the DSP-based ASIC market. Currently, TI's strategy in this area is centered around the TEC320C52, which combines a 0.8-micron, 15,000-gate gate array with TI's popular 16-bit, fixed-point TMS320C52 DSP. The 'C52 is backward-compatible with TI's earlier generations of DSPs (the 'C2x and 'C1x families). Although this means that the architecture is somewhat awkward, it also means that the 'C52 can easily run a wide variety of existing software. The 'C52 includes 1K×16 of data RAM, 4K×16 of program ROM, two serial ports, and a 16-bit timer. It is a very strong competitor on the basis of price/performance and power consumption.

The use of gate-array technology brings customized DSPs into reach for designers of medium-volume applications. For high-volume applications, TI works with its customers to create customized versions of the DSP core, for example, adding or trimming memory and peripheral interfaces.

TI's main U.S. competitors (Analog Devices, AT&T, and Motorola) also have the ability to customize their standard processors for high-volume customers, but none of these vendors has pursued a wide-ranging DSP core strategy, as TI has with the TEC320C52.

SGS-Thomson Focuses on DSP Cores

Whereas TI's DSP core business is a complement to its huge standard-processor business, SGS-Thomson Microelectronics (Lincoln, Mass.) has based its entire

DSP strategy on DSP-based ASICs; it does not sell standard DSPs except as a development aid for customers intending to design ASICs. SGS-Thomson's first DSP core offering, the ST18932, is a 16-bit fixed-point processor. This processor is unique among DSPs in that the same set of arithmetic instructions can process real, complex, or double-precision real operands, as selected by mode bits. ASICs based on the 18932 have been used in a range of highly integrated applications, including personal computer sound cards. The processor suffers from several drawbacks, however, including an unusually obscure assembly language syntax and an unconventional off-core memory interface.

SGS-Thomson's latest DSP core, the ST18950, corrects many of the 18932's faults. Slated for volume production in early 1995, the 18950 is also a 16-bit fixed-point DSP; it is aimed at high-performance, low-power applications such as digital cellular telephones. The processor is built around a 16×16→32-bit multiplier, a 32-bit ALU (which can perform 40-bit addition and subtraction) with two 40-bit accumulators, and a barrel shifter. The core provides three separate buses: one for instructions and two for data. Each bus is 16 bits wide and has an address space of 64K words. The multiple buses support three memory accesses per instruction cycle, and all are expandable off-core.

The 18950 instruction set provides a good variety of instructions for DSP applications, including move/transfer, ALU and MAC (multiply-accumulate) operations, bit manipulation, branches and subroutine calls, hardware looping (nested up to three deep), and stack manipulation. In addition, the 18950 has special instructions to communicate with a user-designed coprocessor: these instructions assert control signals to give the coprocessor an early indication that a communications instruction will be executed. On-chip emulation is supported with a JTAG-compatible interface.

SGS-Thomson plans to complement the 18950 core with a library of compatible peripheral macrocells, including a DMA controller, an interrupt controller that supports up to eight vectored interrupts, and a bus-switch control unit that multiplexes the core's three buses into a single off-chip bus with appropriate control lines, so a single off-chip bus can be used for access to any of the three memory spaces. Additional peripheral cells are planned for the future.

The 18950's performance target is 40 native MIPS with an 80-MHz clock when fabricated in 0.5-micron, 3.3-volt CMOS. SGS-Thomson expects first silicon by 3Q94, and the first production chips in 1H95. The 18950 occupies 10 mm^2 in 0.5-micron CMOS technology.

Licensable Cores Offer a Quick Entrance

A few vendors are taking a completely different approach to the DSP core business. These firms have developed DSP core designs that they license to semiconductor vendors, along with development tools, complementary peripheral macrocells, and technical support. This revolutionary approach offers anyone with access to IC fabrication capabilities an instant way to enter the DSP business, at a cost much lower than that required for the development of a new processor and supporting infrastructure; license fees typically range around $1 million. Semiconductor vendors that license a DSP core can create standard products for internal use or for sale to outside customers, or they can provide a DSP-based ASIC capability to their customers.

The largest supplier of licensed DSP core designs is DSP Group (Santa Clara, Calif.), which introduced its first licensable DSP core, dubbed Pine, in 1992. Recently, DSP Group announced its second-generation DSP core, called Oak, which expands the capabilities of its earlier core.

Pine is a 16-bit fixed-point DSP core aimed at low-power, low-cost applications such as pagers and answering machines. Pine's data path centers around a 36-bit ALU and a 16×16→32-bit multiplier. Pine provides two buses (X and Y) for data manipulation and a third bus for instructions. All use 16 bits of address, except for the Y data bus, which has 11 address bits. Pine's X and Y memories can contain up to 2K×16 RAM or ROM within the core itself, and X memory can be expanded off-core up to 62K×16; Y data memory is not expandable. Program memory is contained off-core. Pine performs at 40 native MIPS with a 40-MHz clock, using either 5.0- or 3.3-volt, 0.8-micron CMOS.

Oak, also a 16-bit fixed-point DSP core, targets higher-performance low-power applications such as digital cellular telephony. Although Oak is similar to Pine in many ways (for example, both have similar 16-bit data paths, and both have identical memory architectures), Oak increases Pine's performance through a number of architectural enhancements. One of the most important improvements is the addition of a bit manipulation unit, which consists of a barrel shifter, bit-field operation logic, and two additional 36-bit accumulators. New instructions in Oak include flexible maximum and minimum instructions (which improve performance on Viterbi decoding); bit-field set, clear, toggle, and test; stack manipulation; signed/unsigned multiplication; and exponent detect and normalize.

Additional improvements include support for double-precision arithmetic, improved interrupt support via shadow registers, and single-level nestable hardware looping. Oak also provides several features for support of code generated by C compilers, including a software stack and an indexed addressing mode.

With both Pine and Oak, DSP Group makes its

complete design database available to licensees. This database includes a synthesizable Verilog HDL model for the core, a cell library, physical layouts, and timing simulations. The licensee then incorporates the core into the ASIC technology of its choice.

DSP Group expects first silicon for Oak in August, with licensees beginning volume production of the first Oak-based ASICs in early 1995. The firm expects Oak to occupy 8.4 mm^2 in 0.6-micron CMOS, excluding any memory. Performance targets are 40 native MIPS using a 40-MHz clock in 0.6-micron CMOS with nominal supply voltages from 3.0 to 5.0 volts. (Although this is the same speed as Pine, Oak has a more capable instruction set and data path.)

DSP Group has announced five Oak licensees to date: Siemens, Integrated Circuit Systems, VLSI Technology, Plessey Semiconductors, and Silicon Systems.

Clarkspur Offers Tiny Cores

Clarkspur Design (Saratoga, Calif.) has been designing DSP cores since 1988 and was the first to offer a DSP core under license. Its first core, the CD2400, uses 16-bit fixed-point arithmetic and a 16-bit instruction word. Based around a 16×16→24-bit multiplier, a 24-bit accumulator and ALU, and two 256×16 banks of data RAM, the 2400 performs at 10 native MIPS. Although not particularly fast, the 2400 is small: 12 mm^2 in (antiquated) 1.5-micron CMOS including its 512×16 RAM, or about 6 mm^2 without memory.

This size is comparable to that of some cores fabricated in much smaller processes today. On the other hand, the 2400 is a simple processor and lacks a number of features that have become standard in DSPs, such as hardware looping and guard bits. In fact, the 2400's 24-bit accumulator is less than twice the width of its data word size (16 bits). This is unusual for DSPs, and implies a significant loss of precision for many DSP operations.

The 2400 is intended primarily for the fax-modem market, although it has seen use in other applications as well. Licensees of the 2400 include Intel, Cirrus Logic, Samsung, Ricoh, and Zilog. Zilog's Z86Cxx and Z89Cxx family DSPs are based on modified versions of the 2400 core; several of the Zilog chips also include a Z8 microcontroller core (see MPR 9/4/91, p. 1).

Clarkspur's latest core is the CD2450. Backward-compatible with the 2400, the 2450 uses fixed-point arithmetic and 16-bit instruction words. A unique and powerful feature of the 2450 is that the core is available with data word sizes ranging from 16 to 24 bits, allowing the ASIC designer to choose the most appropriate data width for his or her application. Because the data width has a strong influence on the core's size and power consumption, this adaptability can be a strong advantage.

The 2450's two banks of data RAM can vary from 256 to 2K words, and the 2450 increases the 2400's accumulator and ALU width to twice the data word size. Other enhancements include support for double-precision arithmetic, bit-manipulation instructions, and the ability to write data to program RAM. Target performance is 50 MIPS with a 50-MHz clock for versions with data word widths from 16 to 24 bits. Current 16-bit samples run at 50 MIPS, and 24-bit samples run at 45 MIPS, according to the company. Silicon area for a 16-bit version of the 2450 (not including RAM) is 3.9 mm^2 in 0.8-micron CMOS.

Tools for Core-Based Designs

Although DSP-based ASICs can combine the best features of custom hardware and programmable processors, they can also bring together the worst problems of each domain, particularly when it comes to design techniques and tools. For example, designing a custom chip containing a DSP requires that hardware and software be integrated before the chip is fabricated, since this is typically the only way that the ASIC design can be verified. For several years, more widespread use of DSP-based ASICs has been held back by lack of adequate tool support.

Recently, however, three of the major ASIC design tool vendors—Cadence Design Systems, Mentor Graphics, and Synopsys—have all made moves in the direction of supporting this type of design. For example, at the Design Automation Conference in June, Mentor Graphics demonstrated, using TI's TEC320C52, a prototype high-level design environment for DSP-based ASICs. Mentor's demonstration showed how an engineer might design a custom coprocessor to reside on the ASIC with the DSP, off-loading the DSP from parts of the application that aren't well matched to the processor's capabilities.

Similarly, Synopsys and Cadence have both demonstrated design support for DSP cores. Through Synopsys' Cossap tool and Cadence's SPW product, both companies have demonstrated the ability to simulate the interactions between programs executing on a DSP core and custom hardware residing outside of the core. This kind of hardware/software co-simulation is a key capability for designing DSP-based ASIC.

Competing Cores Offer Different Strengths

Some of the features of the DSP cores discussed above are summarized in Table 1. The different cores embody contrasting philosophies and each has different strengths and weaknesses. For example, both Texas Instruments and SGS-Thomson use their cores to induce people to build ASICs using the vendor's fabrication facilities. Through the TEC320C52's gate array, TI hopes to make DSP-based ASICs available to lower-volume

Vendor	Core	Year Introduced	Data Width	Accumulator Width	Native Speed	Core Area	Feature Size	Available for License
Clarkspur	CD2400	1989	16 bits	24 bits	10 MIPS	approx. 6 mm^2	1.5 µm	Yes
Design	CD2450	1994	16–24* bits	32–48 bits	50 MIPS	3.9 mm^2	0.8 µm	Yes
DSP	Pine	1992	16 bits	36 bits	40 MIPS	8.2 mm^2	0.8 µm	Yes
Group	Oak	1994	16 bits	36 bits	40 MIPS	8.4 mm^2	0.6 µm	Yes
SGS-	ST18932	1990	16 bits	32 bits	20 MIPS	20 mm^2	0.8 µm	No
Thomson	ST18950	1994	16 bits	40 bits	40 MIPS	10 mm^2	0.5 µm	No
TI	TEC320C52	1994	16 bits	32 bits	40 MIPS	—†	0.8 µm	No

Table 1. An overview of DSP cores. The core area shown does not include memory (except for the ST18932, which contains 384×16 on-core RAM). *The ASIC designer can configure the CD2450's data path to any width between 16 and 24 bits at design time. †The TEC320C52 is an IC containing a TMS32C52 DSP and a gate array with 15K gates of usable logic; TI has not disclosed the silicon area for the 'C52 core.

customers by offering a standard DSP with memory and peripherals and allowing the customer to specify only external logic. Of course, TI can still perform more extensive customization for higher-volume customers (as can Analog Devices, AT&T, and Motorola, despite their lack of a widely marketed core strategy). SGS-Thomson takes a more flexible approach, providing the core as a macrocell in its standard ASIC design flow. Users must specify the DSP's on-chip memory, as well as peripherals and custom logic.

On the other hand, both DSP Group and Clarkspur's cores are licensable, meaning that the user selects the fabrication facility. A key strength of this approach is that the licensee has complete control over the core and can even modify the core architecture if desired. Additionally, licensees that are ASIC vendors can incorporate the cores as cells in their standard ASIC design flow.

Architecturally, the cores differ as well. For example, the Clarkspur 2450 was designed with a "minimalist" philosophy that eschews specialized DSP features (such as hardware looping) in favor of simplicity and small size. Although the lack of features increases programming difficulty and development cost, Clarkspur claims it reduces overall system cost by decreasing the unit cost of each chip. Certainly the 2450's die size (approximately 4 mm^2) is less than half that of its closest competitor.

In contrast, DSP Group's Pine and Oak cores, SGS-Thomson's 18950, and Texas Instruments' C52 are more sophisticated. All ease development through special instructions and more powerful data paths, features that also improve performance for certain applications. Of these three vendors' core offerings, Oak and the ST18950 are the most advanced and have roughly equivalent architectures.

Core-Based ASICs Sometimes Unbeatable

DSP-based ASICs combine the performance and low cost of custom hardware with the flexibility of standard DSPs. For many high-volume applications, this is an unbeatable combination. Core-based designs are just now beginning to blossom, in large part due to a confluence of IC fabrication technology, a critical mass of industry design expertise, and improved design tools. By the end of the decade, a large percentage of high-volume embedded systems that use signal processing will be based on DSP core technology. This will benefit core vendors, ASIC vendors, and, of course, designers incorporating cores into their chips. ♦

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