LSI Builds Custom CPU for Sony PlayStation

CoreWare Program Builds Single-Chip Game Machine from R3000

by Linley Gwennap

Gaining a major design win for its CoreWare program, LSI Logic has developed a MIPS-based chip that will power Sony's forthcoming PlayStation game system. The custom chip, which LSI does not plan to market to other companies, combines a 34-MHz R3000 CPU with a graphics coprocessor, video-decompression logic, and system logic to create a highly integrated, low-cost solution. The design uses LSI's new 0.5-micron CMOS process and contains about one million transistors, combining custom and standard-cell design techniques.

As Figure 1 shows, the R3000 core (including the register file and cache controller) takes just 15% of the die area. The CPU has single-cycle access to the 4K instruction cache and 1K of data memory that are on the chip. It connects to the other devices on the chip through a 132-Mbyte/s bus. The 3D-transformation coprocessor contains its own multiply-accumulate hardware and uses a dedicated 32-bit bus to transfer data to an external graphics chip. Sony claims that these two chips together can draw 360,000 texture-mapped polygons per second, generating high-quality images at 30 frames per second. This graphics performance exceeds that of current low-end workstations.

The independent video-decompression engine decodes images in motion JPEG format with up to 24-bit color. It uses DMA to read data from the CD-ROM and write the decompressed results into main memory.

The chip also integrates an extensive set of system logic. A seven-channel DMA controller supports the three autonomous processors by moving independent data streams into and out of the chip. The built-in DRAM controller connects to the memory subsystem using a 32-bit bus. A separate 16-bit bus supports slower I/O devices like the external sound chip. Finally, the design includes three 16-bit counter/timers and serial I/O.

Sony has not yet announced the PlayStation, which it expects to begin shipping in the U.S. early next year as part of the crowded high-end game market. The PlayStation, which will sell for less than $400, will compete with the SegaSaturn system, which uses two SH7604 chips *(see **080203.PDF**)*; Nintendo's forthcoming MIPS-based system *(see **0712MSB.PDF**)*; and the ARM-based 3DO machine *(see **0701MSB.PDF**)*.

The LSI chip provides a more integrated solution than any of these, reducing cost and system power. The R3000 nearly doubles the performance of the ARM or of a single SH7604. Nintendo is rumored to be using a derivative of NEC's R4200 in its 64-bit game machine. The R4200 offers more performance than the R3000 CPU core but will be hard pressed to match the combined performance of the CPU, graphics, and decompression engines on the LSI chip. Nintendo must add considerable logic to its R4200 derivative to match the feature set of the LSI chip.

LSI did not reveal the die size of the part but we estimate it to be about 64 mm^2, resulting in a manufacturing cost of roughly $20 according to the MPR Cost Model *(see **071004.PDF**)*. This cost is much less than that of the two 7604s used in the SegaSaturn and about half that of the basic R4200, which could increase in cost if Nintendo adds features.

This design win—the first by a U.S. company in a next-generation game machine—is a strong endorsement of LSI's design ability. Sony has its own MIPS core *(see **071506.PDF**)* but chose LSI because of its more complete portfolio of CPU, graphics, and JPEG function blocks. The CoreWare program allowed LSI to deliver a product quickly, accelerating Sony's development cycle. This chip—and products such as Motorola's 68356 *(see **080802.PDF**)*—illustrates how embedded CPU vendors with broad technology portfolios are better positioned for high-volume design wins. ♦

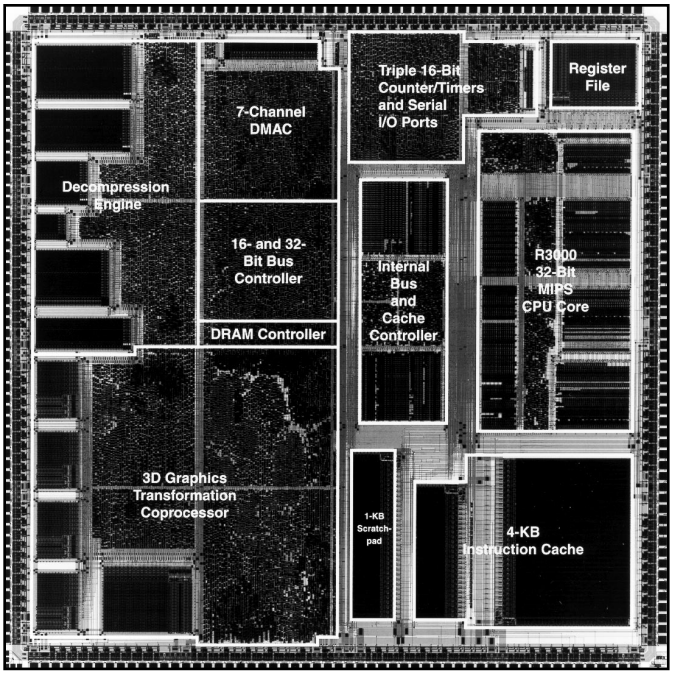

Figure 1. The custom CPU for the Sony PlayStation uses LSI's 0.5-micron, three-metal-layer CMOS process and contains about one million transistors. LSI did not reveal the die size.

