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Zilog Introduces 32-bit Z80 to U.S.

Quadruple Register Sets Speed Context Switching

by Curtis P. Feigel

Moving into the 32-bit age, Zilog's new Z380 is the first major leap forward in the Z80 architecture in seven years. The new processor executes most instructions in two cycles, which, coupled with its higher clock speed, gives it an order of magnitude more performance than the original Z80, first released in 1977.

Although it is an extension of the venerable Z80 architecture, the Z380 is substantially different inside. It incorporates four complete 32-bit register sets to facilitate context switching, has a 16-bit external data bus, and allows 4G of address space. It can also run Z80 code using a compatibility mode. The Z380 has been shipping to Japanese customers for about a year but was only recently announced in the United States.

Why the company chose to release the product in this way is not entirely clear. Zilog claims that, because development tools and support were not in place until recently, the Z380 was unattractive to U.S. customers. By implication, it seems that Zilog had a ready market for the part in Japan that did not require substantial development support.

Japanese chip manufacturers, such as Hitachi and Toshiba, have supported the Z80 architecture since the late 1970s. They have a history of extending and refining the design, using different fabrication technologies, and developing versions with faster clock speeds, wider data paths, more registers, integrated peripherals and interfaces. Zilog itself fields several dozen chips built around the Z80 architecture, offering a broad spectrum of integrated peripherals at prices from moderate to downright cheap: street price for a low-end Z80 CPU is about $1. Many systems can be implemented with just the processor chip and memory.

Despite its age, the Z80 continues to be successful, shipping (according to Zilog) over 30 million units per year—not counting processors built by licensees. This puts the Z80 family on par with Motorola's 68000 line, which Dataquest says shipped 36 million units in 1993.

Licensees Spread the Faith

A number of alternate sources exist for Z80-type processors including Sharp, SGS-Thompson, Texas Instruments, Toshiba, and Goldstar. Zilog has displayed a willingness to license the architecture and help other companies develop Z80 variants, and even to acquire enhanced Z80 designs and bring them into the Zilog product line. The Z180, for example, began as Hitachi's 64180. Sharp, Toshiba, and VLSI Technology offer Z80-architecture processors as megacells for use in ASIC designs.

Table 1 (see below) shows how the new device fits into the range of Z80-derived processors. The original Z80 uses 8-bit registers, which can be paired to hold 16-bit values, and an 8-bit datapath. Most instructions require four clocks to complete. Early designs implemented each function as a discrete chip: the processor, DMA control, counter/timers, serial- and parallel-I/O controllers, etc. NMOS was the first fabrication technology, but the design was later transferred to CMOS. Discrete Z80 processors, in both CMOS and NMOS, are still available and, according to Zilog, account for over half of total Z80 sales.

Announced in 1987, the Z180 integrates the CPU, DMA, counters, serial I/O, and an MMU on one chip. It also adds a new multiply instruction. The MMU allows external memory to be as large as 1M but performs bank switching to maintain compatibility with the architecture's original 64K space. That is, it maintains the 64K address limit, but uses it as a window into a much larger 1M space. The Z180 requires three clocks per instruction. A fully static variant, the S180, is available. Z180-class devices are a popular choice for fax/modems and other communications devices due to their high level of integration and low cost.

The Z280, also announced in 1987, is Z80-compatible but more heavily pipelined, with 16-bit registers and datapath. It incorporates a 256-byte fully associative instruction cache and an MMU. It is limited to a 64K physical address space but allows 16M of virtual addresses.

The Z280 supports separate instruction and data spaces and has user and supervisor privilege modes. The company is deemphasizing the Z280's role in the family and encourages designers to skip directly from the Z180 to the Z380.

Z380 Includes 32-Bit Registers

The new Z380, shown in the die photo in Figure 1, is a fully static design that can run at 18 MHz at 5 V and 10 MHz at 3.3 V. Its Z80 register set is extended to 32 bits. The execution unit uses a four-stage pipeline and incorporates a prefetch queue. The design adds a stack-pointer-relative addressing mode.

As shown in Figure 2, the Z380 contains an on-board refresh controller. It performs CAS-before-RAS refresh at a software-selectable rate. This is a step up from the simple refresh counter incorporated in earlier versions. Six chip-select outputs each have a programmable number of wait states. The incoming interrupt lines can each be used as dedicated request lines or combined as a vectored interrupt. The Z380, like the Z80, distinguishes between memory and I/O space, so the bus interface has separate control signals for each. The instruction set contains instructions specifically to access I/O space.

The Z380 is the first Z80-type processor that can access more than 64K of memory in a linear fashion and without an MMU or a banked memory. This is achieved simply by extending the size of the address registers.

	Z380	Z280	S180	Z180	Z80
Introduction Date	1994	1987	1992	1987	1977
Supply Voltage	3.3 V, 5 V	5 V	3.3 V, 5 V	5 V	5 V
Clock @ 5 V	18	10, 12	33	6, 8, 10	6, 8, 10, 20
(MHz) @ 3.3 V	10	n/a	20	n/a	n/a
Address Bus Size	32	24	20	20	16
Data Bus SIze	16	16	8	8	8
Register Sets	8	2	2	2	2
Instruction Cache	none	256 bytes	none	none	none
Timers	none	3	2	2	none
Serial Ports	none	1	3	3	none
Interrupts	4 IRQs	1 IRQ	3 IRQs	3 IRQs	2 IRQs
DMA Channels	none	4	2	2	none
MMU	no	yes	yes	yes	no
Package	100 QFP	68 PLCC	64 DIP 80 QFP 80 PLCC	64 QFP 80 PLCC	40 DIP, 44 QFP, 44 PLCC
Clocks/Instruction	2	3	3	3	4
Relative Speed	3.6	1.5	1.1	1.1	1.0
Price (1,000s)*	$11.75	$22	$9.40	$4.90	$4.00

Table 1. By reducing the number of clock cycles per instruction, the new Z380 gains a significant speed advantage over its Z80 siblings. (Source: Zilog)
*Price given for highest-speed version of each processor.

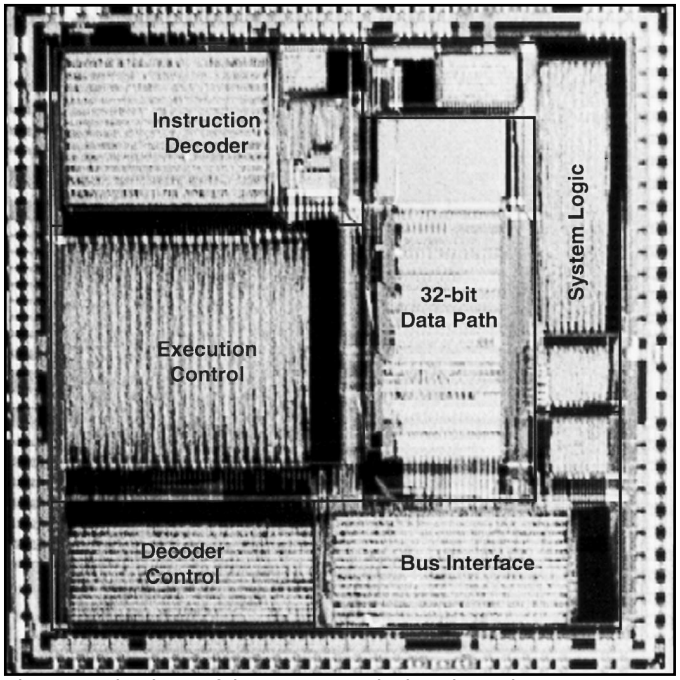

Figure 1. Die photo of the new Z380 device shows its 115,000 transistors on an 86 mm^2 die built in a 1.0-micron, two-layer-metal CMOS process.

Under typical conditions, the chip dissipates 50 mW at 5 V and 18 MHz, and just 12 mW at 3.3 V and 10 MHz. In its low-power sleep mode (entered by executing the sleep instruction), its oscillator circuitry runs, but very little of the device's circuitry is clocked, so power consumption drops to 100 µW. In standby mode, the oscillator stops and must be restarted before program execution can continue.

The Z380 is now built in a 1.0-micron, two-layer-metal CMOS process. Zilog plans to shrink the processor to a 0.8-micron process that could allow the device to run as fast as 40 MHz. The company expects that samples of this device may be available as early as 1Q95.

Wide Processor Is 8-Bit Compatible

The new Z380 is opcode compatible with the Z80 and Z180, and it can execute without modification programs intended for those processors. In addition, it supports word (16-bit) and longword (32-bit) data modes. In the Z80 mode, the program counter and stack operations work on 16-bit addresses. This mode is fully compatible with the Z80's 64K address space. When software enables extended mode, the program counter and stack operate on 32-bit quantities, giving access to 4G of memory and 4G of I/O space. The device always drives all 32 address bits onto the external bus. In Z80 mode, the 16 most-significant bits of the extended registers are set to zero, so any register value that is put on the bus will cause the bus's two high-order bytes to be zero.

The original Z80 architecture has two sets of registers (one called the primary set and the other the working set). This allows programs to maintain two machine

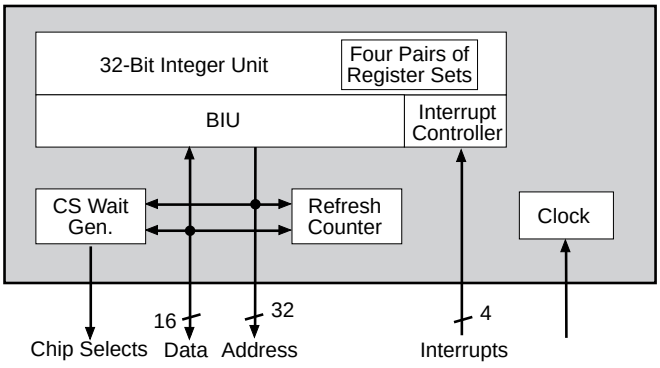

Figure 2. The straightforward design of the Z380 includes few peripherals but incorporates glue logic, such as chip selects and a DRAM refresh counter, to simplify its integration into a system.

states in the registers during, say, interrupt handling. In other processors, this must be done by saving the register file's contents to memory. The contents must then be reloaded to the registers once the interrupt had been handled. Being able to perform a context switch without the memory access simplifies and speeds context switching and interrupt handling.

As Figure 3 shows, the Z380 carries this concept a step further: the complete pair of register sets is replicated four times. A register set is designated as the working set by setting appropriate bits in the processor's Select register. Each set contains an 8-bit accumulator (A), a flag register (F), and six 8-bit general-purpose registers (B, C, D, E, H, and L).

The accumulator is the destination register for 8-bit math and logic operations. The six general-purpose registers can be paired (as in the Z80), forming three 16-bit registers: BC, DE, and HL. In extended mode, these 16-bit registers become the low-order half of the larger 32-bit register set: BCz, DEz, and HLz. Or the high-order bytes can be accessed using the SWAP instruction or word load instructions.

The four index registers (IX, IX', IY, and IY') are also extended to 32 bits. Only one register of the four can be the active index register at any given time. Although data in the inactive registers can still be accessed, so they can function as general-purpose registers, each byte must be accessed individually.

Performance Is Offset by Low Cost

Zilog was unable to provide standard benchmarks such as Dhrystone numbers. For comparing against other processors, it uses a hand-tracing technique on selected code fragments from typical embedded applications. This technique requires calculations to determine the number of clocks each processor needs to execute the fragment. The procedure involves making numerous assumptions, including how memory and cache react and how data is aligned. Table 2 shows the results.

Price & Availability

The Z380 is available now at $9.99 in 100,000-unit quantities or $11.75 in 1,000-unit quantities. For further information, contact your local Zilog sales office or contact Zilog's U.S. headquarters (in Campbell, Calif.) at 408.370.8000; fax 408.370.8056.

According to Zilog's calculations, the 960KA has the largest code size but requires the fewest clock cycles to execute that code. (The 960SA uses the same CPU core as the 960KA but has a 16-bit external bus similar to the Z380, making it a more logical choice for comparison.) On a clock-for-clock basis, the Z380 is about 40% slower than the 960 in overall execution speed. The Intel part is available in speeds up to 25 MHz, while the fastest Z380 currently is 18 MHz.

The 960 and Z380 both have multiple register sets, but the 960 has hardware and microcode that automatically swap the contents of a register set to RAM when necessary. From the software perspective, this is a more flexible solution than the Z380's multiplicity of register sets. If the Z380's register-set capacity were exceeded by deeply nested interrupts, for example, explicit code would be required to swap the register contents to RAM. The two processors exhibit similar performance on Zilog's interrupt test, which may not exercise the devices beyond this limit.

Motorola's 68020 appears to be a fair match for the Zilog part. The Z380 is somewhat slower on the Multi-

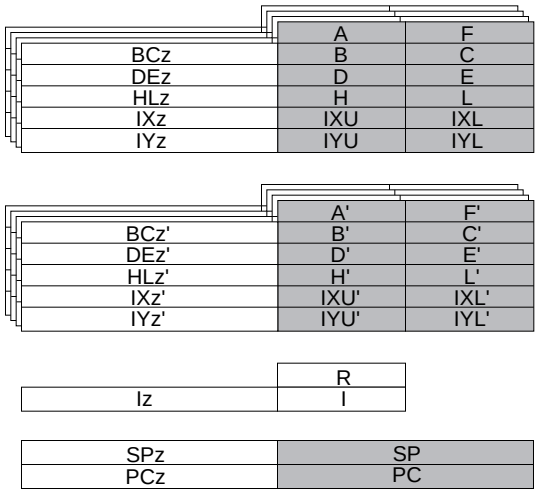

Figure 3. The extended register set of the Z380 allows grouping of 8-bit-wide and 16-bit-wide registers to accommodate 32-bit values. Register names with a "z" suffix refer to the complete 32-bit register line. The design provides four complete register sets to facilitate context switching. In this diagram, shaded portions represent registers present in the original Z80 design.

		Z380	i960KA	68020
I/O Loop	clocks	465	248	440
	bytes	65	120	92
Signed Bytes	clocks	43	31	46
	bytes	52	76	64
Mult/Acc	clocks	254	92	212
	bytes	95	104	54
Interrupt	clocks	133	123	288
	bytes	66	92	80
Block Move (clocks/byte)		2.75	1.25	2.87

Table 2. To compare the Z380 to its competition, Zilog hand-traced sample programs, computing both the code size and the number of clocks each processor would require. Given processors of the same speed grade, Intel's i960 would clearly be faster, but it would also require the greatest amount of memory. (Source: Zilog)

	Z380	i960SA	68EC020
Clock (MHz)	18	16	16
Address Space (bytes)	4G	4G	16M
Data Bus SIze (bits)	16	16	32
Register Sets	4	4	1
Instruction Cache	none	512 bytes	256 bytes
DRAM Support	yes	no	no
Transistors	115,000	350,000	103,000
Die Size	86 mm^2	59 mm^2	38 mm^2
Process Size	1.0 µm	0.8 µm	1.0 µm
Metal Layers	2	2	2
Relative Speed*	1.0	1.6	0.8
Price (1,000s)	$11.75	$12.00	$11.00

Table 3. Although the Z380's price is comparable to leading 32-bit embedded processors, it is outperformed by the more RISC-like i960. *Performance values based on Zilog's figures.

ply/Accumulate test, but the Motorola processor takes over twice as long to complete the Interrupt test, due to its need to save its single register set to memory. Zilog's big advantage is the migration path the Z380 offers for users of its 8-bit processors. Users of Motorola's 6800-series 8-bit processors would have to expend some effort to port code to the 68000 family. One could argue, however, that versions of the 68000 with 8- and 16-bit external buses are still available and are code-compatible with the rest of the 68000 family.

As Table 3 shows, even price—always a major issue in embedded systems—is a tough contest for the Z380 to win. An i960SA with better performance than the Z380 is priced at $12 (in 1,000-unit quantities) compared with the Z380's $11.75. A system built with the Intel part would be somewhat more expensive, however, considering that its larger code size would require more memory.

For designers who want a performance growth path, the 960 family is clearly the winner, as the SA is the low end of the 960 line. Where system cost is the primary concern, Zilog has an edge.

Age Has Its Advantages

Several factors combine to make the Z80 architecture popular in embedded applications: cost, of course, is critical, as are availability and multiple sourcing. But the fact that it has been around for so long is also a selling point. Programmers are familiar with the architecture and the tools, and if the previous version of a product used the Z80, it's far easier to continue with that line than to rewrite old code.

Zilog continues to evolve the 17-year-old architecture, rather than create a new one, because of its customers large investment in software. Many embedded systems use assembly code that would be difficult to port to another processor. Enhancing the architecture allows customers to keep a short design cycle by capitalizing on their existing code base. For these reasons, Z80-type devices are likely to continue to be found as the controller in numerous computer peripherals such as modems, disk drives, and low-end impact or inkjet printers.

Although the Z80 architecture may seem old and out of date compared with modern superscalar and RISC designs, in many cases it's the appropriate tool for the job. With its low cost and four register banks, the Z380 is attractive as a microcontroller that needs to handle interrupts and context switches. But the Z380 today has little performance headroom; there are few ways to go if the application needs more power.

It is unlikely that we'll ever again see a Z80 as the main processor in a personal computer, but given the inertia involved in developing software, these chips are bound to be common controllers in intelligent computer peripherals for years to come. The Z380 is a welcome upgrade for existing designs but a less likely choice for new designs, which are attracted to low-end RISC processors and the highly integrated 68300 family. ♦

