Competitors Seek to Counter Pentium Push

Intel's De-emphasis of DX4 Creates Opportunity for Enhanced 486s

by Michael Slater

As Intel prepares for an all-out push to shift the mainstream PC market from the 486 to Pentium, its competitors are preparing enhanced 486 chips that could prolong the life of that family.

Intel's de-emphasis of the DX4 in desktop systems *(see **0806MSB.PDF**)* has left an opening for others to exploit. Major PC makers, such as IBM and Compaq, apparently will be able to get DX4-100 processors for desktop systems, but smaller PC makers—as well as embedded users and makers of upgrade modules—are out of luck. Intel is taking new orders only from makers of portable systems, and no DX4 chips are being sold through distributors. Unfortunately, none of Intel's competitors will have products to fill this gap until the fall.

AMD K5 Aims at Pentium

Although AMD surely will try to extend the life of the 486, it won't be left out of the Pentium market. At AMD's annual shareholders' meeting, President and CEO Jerry Sanders revealed that the company's forthcoming K5 microprocessor is a four-issue superscalar design using three million transistors. A spokesperson for AMD said that the chip would be pin-compatible with Intel's Pentium and claimed that it would outperform the 100-MHz P54C by at least 20%.

Sanders characterized the chip as using a RISC core but not a RISC instruction set—a claim Intel would also make for Pentium. AMD's four-issue core presumably will provide higher performance than Pentium's two-issue design. AMD now calls the K5 the first member of the K86 family, a name created to distinguish the company's independent designs from its current products, which are modified Intel designs.

First silicon of the K5 is promised for late this year, using 0.5-micron wafers from the company's Submicron Development Center. Volume production will come from Fab 25, which is scheduled to begin running wafers by the end of this year and be in volume production by the middle of 1995. AMD's goal is to have the K5 ready for volume production at that time. Fab 25 is expected to process 5,000 wafers per week by 3Q95.

AMD also said that the K6 and K7 processors would follow relatively quickly behind the K5, appearing in 1996 and 1997, respectively. The K5 and K6 are being developed in parallel. AMD expects the K6 to match Intel's P6, possibly shrinking the generation gap between the two companies to less than a year.

AMD Plans Enhanced 486 Line

Intel's DX4 has left AMD a step behind in the 486 market, but AMD plans to introduce clock-tripled 486 chips by year-end. The company has not revealed details of its plans, but its presentation at last year's Microprocessor Forum hinted that a 16K, write-back cache version is in the works. Intel's DX4 uses a write-through cache, and a write-back design would gain a small performance advantage. The larger cache, as well as higher clock rates, will be made possible by AMD's 3.3-V, 0.55-micron "CS24" process. AMD showed 486 chips fabricated in the new process at Comdex last fall.

AMD plans to differentiate its products on clock rate as well. The first such offering will be a 486DX2-80, due in the third quarter, which probably will not include an enhanced cache. This chip provides an upgrade for system designs based on AMD's 486DX-40, a device that Intel has not offered. A 100-MHz part is expected to follow by year-end. AMD reportedly also plans to ship a clock tripler for the 40-MHz socket, delivering 120-MHz on-chip performance, but this product isn't likely to appear until 1995. Intel has not revealed any plans to take the 486 beyond 100 MHz and, given its focus on shifting the market to Pentium, is unlikely to do so.

Last week, AMD introduced a minor upgrade to its 486 line. Its 486SX, DX, and DX2 chips are all now available in "L" versions, which add system-management mode features for power management. (Intel already provides SMM in all its 486 processors.) These features have previously been available from AMD only in 3.3-V 486 chips but are now offered throughout the line in support of "green" desktop systems. There is no price premium for the "L" versions, which essentially replace the previous designs.

AMD's SMM design follows the architecture used in the company's 386 chips, which is somewhat different from Intel's SMM but provides equivalent functions. Several system logic makers already provide chip sets supporting AMD's SMM.

Cyrix to Exploit IBM Process

Cyrix is reworking its 486 processor design for IBM's 0.6-micron process. At the same time, the company could double the cache and add a clock tripler, bringing it into the DX4 arena. Cyrix may also take this opportunity to enhance its CPU core, which isn't quite as fast as Intel's 486 at the same clock rate, making it hard to compete at the high end of the market.

IBM has its own Blue Lightning design, which is already shipping at 100 MHz and matches the DX4's 16K cache. So far, however, IBM has not mated this core to a 486 bus interface, which limits its performance.

Cyrix may also mate its forthcoming M1 core to a 486 pinout, which could provide a high-performance upgrade for 486 system designs.

Intel Using Price to Push Pentium

According to information obtained by *PC Week*, Intel has quoted customers volume prices of $370 for a Pentium-60 by the end of the year, with 66-MHz chips falling to $472 and 90-MHz devices dropping to $625. (Today's 1,000-piece prices are $675 for 60 MHz, $750 for 66 MHz, and $845 for 90 MHz.) These steep price drops will make it harder for high-end 486s to hold their ground, pushing their prices down to the sub-$300 level. By aggressively cutting the Pentium-60 price, Intel can make this chip more attractive than the DX4-100, priced at $580 today.

With increasing 486 competition (including new chips from UMC) *(see **080702.PDF**)* and Intel's aggressive pricing of Pentium, 486 prices are likely to drop rapidly by the end of the year. By the end of 1995, the 486 probably will look like the 386 in 1992, with Intel all but dropping out of the market but others shipping many millions of chips. ♦

Bug Fixed in Cyrix's 486DX

An obscure but potentially serious floating-point bug has been uncovered in Cyrix's early 486DX and DX2 chips. The bug affects only a few thousand chips shipped between October of last year, when the products were introduced, and this March, when the bug was corrected in a revision to the chip's design.

The bug was uncovered by Ed Curry, proprietor of a small, independent testing lab called Lone Star Evaluation Laboratories (Georgetown, Texas). Curry has been testing 486 microprocessors from all vendors to collect data for a compatibility report he plans to publish this summer. The bug was uncovered by a floating-point test routine, compiled using IBM's OS/2 C compiler, that Curry expected would show minor differences in floating-point algorithms. Instead, the Cyrix chips produced completely erroneous results.

According to Dave Methvin at *Windows* magazine, who first reported on the bug, the failure occurs when a MOV instruction that loads a register from memory is followed by the FCLEX instruction, which clears the floating-point status register. If the memory location referenced by the MOV instruction is in the on-chip cache, everything works fine. But if the MOV requires an external bus cycle, the FCLEX instruction aborts the cycle and the register that is the target of the load ends up with the wrong data.

Cyrix downplays the significance of the bug, and a spokesperson even claimed that they don't consider it to be a bug. Their support for this claim is that their standard of compatibility is the operating systems and applications used in PCs, and the bug has not been shown to cause a problem in any off-the-shelf application. It occurs only in 32-bit mode, so it could not be triggered by most PC applications. Software compiled for the 386 inserts an FWAIT instruction before any floating-point instruction, so the problem affects only code compiled explicitly for 486 and later processors.

Despite Cyrix's claim, this is clearly a bug: when an instruction fails to produce the result that anyone would expect, there can be no other name for it. It is true that it is known to have been triggered only by a piece of test code, but it is entirely possible that someday a commercial application—or a custom application written by a PC user—will trigger it. Even if no compilers generate the offending sequence (and Cyrix says that IBM has changed its OS/2 compiler to ensure this), there is nothing to prevent an assembly language programmer from stumbling across it.

The insidious thing about this sort of bug is that the application will simply produce the wrong result, probably with no indication that anything has gone wrong. Although it is unlikely that any of the few thousand chips shipped with the bug will ever encounter software that could trigger it, Cyrix should notify customers that the bug exists and offer to exchange any CPU that has the bug with a corrected one. There is no indication that Cyrix plans to do so.

