Hitachi Extends SH7000 Line at Top, Bottom

SH7604 Is First Announced Microprocessor with SDRAM Interface

by Linley Gwennap

Building momentum for its SH7000 family, Hitachi plans to deliver several new parts this year. The company has already won a spot in Sega's forthcoming 32-bit game machines for its SH7064, the first of its second-generation (SH-2) parts. Hitachi rates this chip as 60% faster than its current SH7000 processors; the company plans to sample the SH7604 in Japan by 2Q94. The 7604 is the first SH part with an on-chip cache and the first microprocessor of any kind to incorporate a direct interface to SDRAM (synchronous DRAM).

At the other end of the line, Hitachi will downsize the original SH-1 parts with the new 7020 and 7021, which include less on-chip memory and eliminate the A/D converter, reducing cost. The company expects to sample these chips in Japan beginning in March. It is also developing another version, the 7012, with no ROM and no DMA controller, but did not announce sample dates for this device.

As is common with Japanese processors, samples of these products will not appear outside of Japan until about three months after the domestic sample dates. Full production of both the 7604 and the 702x parts is expected by 3Q94. Hitachi has not announced pricing—in yen or dollars—for any of these new products.

New Core Boosts Performance

The 7604 was designed to meet the needs of the Sega game system, which requires better performance than the SH-1 parts have. The 7604 uses the SH-2 CPU core, which runs at 28.5 MHz with a 5-V supply, more than 40% faster than the SH-1 *(see **070802.PDF**)*. This increase was achieved by redesigning the core for higher performance, although the processor remains in the same 0.8-micron process used by the SH-1 chips. This frequency also happens to be four times the 7.14-MHz clock rate used to drive a standard NTSC television set, making it easy for Sega to generate.

The SH-2 core implements the original SH7000 architecture *(see **071103.PDF**)*, a 32-bit RISC design with 16-bit fixed-length instructions. The new core adds the seven new instructions listed in Table 1. The original instruction set includes only non-delayed versions of conditional branches; the new core adds delayed versions as well. Although the former can reduce code size by eliminating NOPs, the non-delayed branch takes three cycles to transfer control. When a useful instruction can be placed in the delay slot, the delayed branch improves performance by branching in two cycles.

All branches in the SH-1 instruction set are PC-relative with a 12-bit displacement. The new core adds two position-independent branches that add a register value to the displacement. These can be used in programs too large for the 12-bit displacement and are also useful for constructing branch tables.

Two new double-length multiply operations were added to support 32-bit arithmetic. The final new instruction will decrement a register and set the "T" flag if the result is zero. This instruction can be used in combination with a conditional branch for a fast loop test.

The 7604 contains a multiply-and-accumulate (MAC) unit that implements the new math instructions with a 32-bit multiplier and a 64-bit accumulate register. A 32 × 32-bit multiply, with either a 32- or 64-bit result, takes two to three cycles on the new chip, the same speed as a 16 × 16-bit multiply on the 703x, which has a 16-bit multiplier. Hitachi believes that the new, wider multiplier is suited to high-quality audio and font transformation in laser printers, but the main objective is to perform the three-dimensional coordinate transformations used in Sega's advanced video games.

The 7604 also contains a hardware divide unit not included in previous SH7000 chips. It can divide a 64-bit value by a 32-bit value in about 37 cycles. The divide unit is implemented as a separate function unit from the CPU; to use it, software must write values into a set of predefined I/O registers and write to the control register to start the operation. The divide unit generates an interrupt when the calculation is complete.

Fast, Low-Power Cache

To further boost performance, Hitachi added a 4K cache to the 7604, replacing the 8K of RAM on the 7032. The cache automatically stores frequently referenced data and instructions, delivering a performance benefit even for programs stored in external ROM. The cache is unified and four-way set associative, improving the hit

Instruction	Description
BRAF	Position-independent unconditional branch
BSRF	Position-independent subroutine call
BF/S	Delayed conditional branch (if T=0)
BT/S	Delayed conditional branch (if T=1)
DMULS	Double-length (32-bit) signed multiplication
DMULU	Double-length (32-bit) unsigned multiplication
DT	Decrement and test register

Table 1. The SH-2 CPU core includes seven new instructions not implemented in the original SH7000 processors.

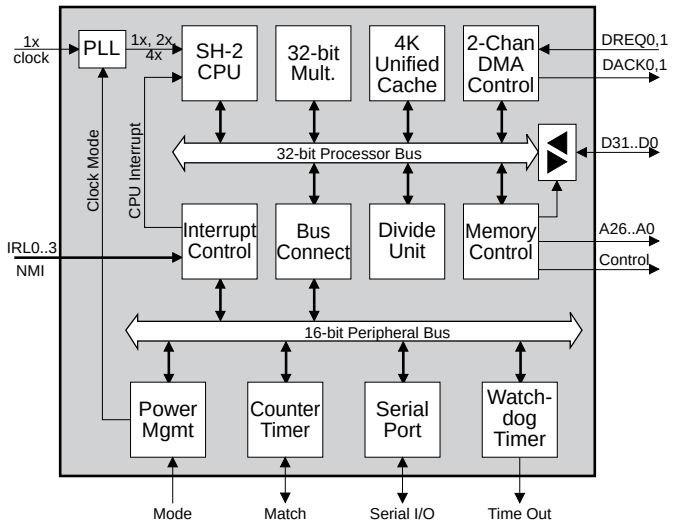

Figure 1. Block diagram of the 7604 shows that the new CPU core connects to a variety of system logic and a serial port.

rate over a direct-mapped organization. The line length is 16 bytes, and the cache uses a write-through protocol. For applications that require a deterministic memory-access time, the on-chip memory can be partitioned as 2K for cache and 2K for main memory.

Even with the on-chip cache, however, the access time to external memory is a critical performance factor, especially for programs with large data sets (such as video games). The 7604 can connect directly to synchronous DRAMs *(see **070205.PDF**)* for maximum performance. The 7604 also uses a 32-bit bus to external memory, twice the width used in the SH-1 chips. The wider bus and fast response time of the SDRAMs allow a 16-byte cache line to be filled in just six cycles (3-1-1-1 access pattern) at 28.5 MHz.

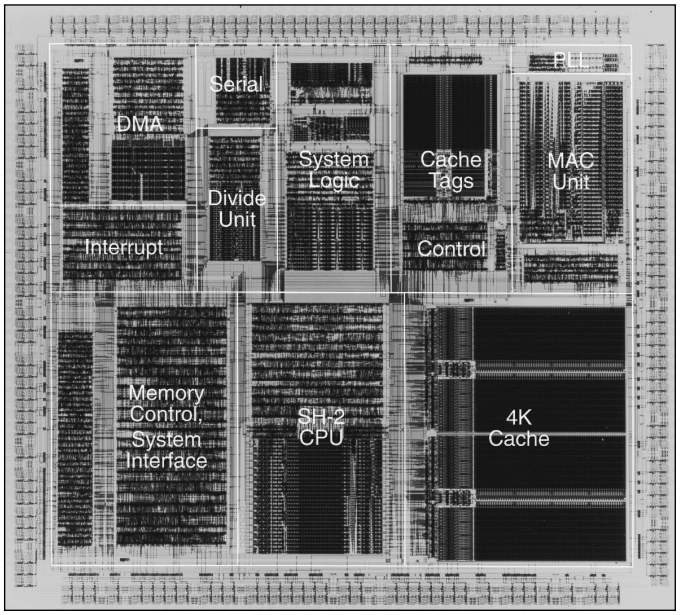

Figure 2. Die photo of the SH7604, which incorporates 450,000 transistors on a 9.52 × 8.66 mm die using 0.8-micron CMOS.

The memory controller supports up to four banks of memory, each with different timing. Thus, with no glue logic, a single configuration could have one bank each of SDRAM, DRAM, pseudo-static DRAM (PSDRAM), and ROM. The 7604 supports burst or standard ROMs. Although the bus width is 32 bits, 16- and 8-bit memories are also supported on a per-bank basis. This allows a low-cost 8-bit-wide ROM, for example, to boot the system while performance-sensitive code is read from DRAM.

The number of banks is reduced from eight in the 703x parts, but the size of each bank is increased to 32M, for a total memory space of 256M.

System Logic on Chip

Like other SH7000 processors, the 7604 contains a complete set of system logic, as Figure 1 shows. This logic is similar to that in the 703x with two exceptions. The 703x implements four DMA channels, while the 7604 has only two. Also, the 703x has eight external interrupt pins, plus NMI; the 7604 multiplexes 16 interrupts onto four pins, plus NMI.

The new chip includes a single serial port much like that on the previous parts. It leaves out the second serial port implemented in the 703x, as well as several I/O devices that are somewhat unusual: the A/D converter, pulse generator, and pattern generator in the 703x. These devices were included in the original 703x parts for VCRs and other consumer applications, but they were omitted from the 7604 to save die area.

The new processor also features a phase-locked loop (PLL) circuit on the clock input. It can provide a 1×, 2×, or 4× clock to the CPU. This allows Sega to use the 7.14-MHz NTSC clock signal to directly drive the processor. The clock multiplier is software-selectable and can be changed on the fly, reducing CPU power when performance is not needed.

Better Performance at No Extra Cost

This multitude of new features increases performance to the level required by the Sega video game and other demanding applications. Taking advantage of the faster clock speed and compiler improvements, Hitachi rates the 7604 at 25 Dhrystone MIPS, a 56% increase over the 20-MHz SH-1 parts. Applications using the 32-bit multiplier and divider may see even greater improvements. The 32-bit bus and SDRAM support will boost the performance of large programs that overflow the 4K cache (unlike Dhrystone).

The new core can operate at 20 MHz using a 3.3-V supply. This speed, combined with the other enhancements, nearly doubles the MIPS rating of the SH-1 core, which tops out at just 12.5 MHz at the lower voltage.

These improvements have not increased the cost of building the chip. In fact, the 7604 die, shown in Figure 2,

is about 10% smaller than the 703x. The larger MAC unit and the new divide unit are offset by the reduced peripheral set. The 4K cache is also smaller than the 8K of RAM implemented on the 7032.

The wider system bus on the 7604 requires a 144-pin PQFP, a bit bigger than the 703x package. The manufacturing cost of the two chips should be about the same: around $20, according to the MPR Cost Model *(see **071004PDF**)*.

The increased performance comes with only a slight increase in power, as Table 2 shows. Like its predecessor, the new chip has a variety of power-down modes, and the variable-speed PLL can trim power consumption when power management is enabled. Finally, the on-chip cache reduces the number of external memory references relative to the 703x, reducing the total system power.

Smaller Parts Cut Manufacturing Cost

The other new processors—the 7020 and 7021—are intended to extend the low end of the SH7000 line. These chips use the the SH-1 CPU core and are very similar to the 703x chips *(see **070802.PDF**)*. The major change is a reduction in the amount of on-chip memory, as Table 2 shows. Hitachi has also removed the A/D converter.

These changes shrink the die by 35%. The elimination of the eight analog input pairs allows the 702x to fit into a 100-pin TQFP package, further reducing cost. As a result, the MPR Cost Model estimates the manufacturing cost of the new chips at $13, one-third less than the 703x (or 7604).

The Fastest Low-Power Processor

Although Hitachi has not released pricing for the new chips, it says that the 7604 will carry about the same price as the current 7032, which sells for $32 in quantities of 10,000. With its significantly lower cost, the 702x could be priced around $20, making it competitive with the ARM600 and other 32-bit embedded chips.

Hitachi's performance measurements show the 7604 to be slightly faster than the ARM7 or 92020S Hobbit processors, based on Dhrystone MIPS. This would give the SH-2 processor the best performance among CPUs for low-power systems, although other vendors may deliver faster parts by the time the 7064 begins shipping. If Hitachi can meet its price goals, the new chip should be competitively priced as well.

At this time, Hitachi is pursuing typical high-end embedded applications—such as printers and factory automation—along with consumer products such as video games and other multimedia devices. The MAC and divide units of the 7064 give it an advantage in products that require intensive audio or video processing. The aggressive price/performance of the new parts, particularly the 702x chips, should allow them to do well in a variety of embedded products.

Price and Availability

Hitachi has not announced any prices for the 7604 or 702x parts. The company plans to sample the 7604 in May, but in Japan only; general sampling is planned for August. Hitachi says it will sample the 702x chips in March, also in Japan only, with general sampling in June. Production of all parts is planned for 3Q94.

For more information, contact your local Hitachi sales office or call Hitachi America at 800.285.1601, ext. 27.

The SH7000 chips are also suitable for some handheld computing devices. Hitachi says that its SH7000 chips will appear in "fixed-function PDAs" (that is, devices with no software expandability) from multiple companies in 1994. The company also claims that a major PDA operating system is being ported to the SH7000 for the SH-3 generation of products, due in 1995. These chips will include an MMU, making them suitable for most popular PDA software.

Hitachi has laid out an ambitious plan to release a new generation of SH7000 processors every year, leading to a 200-MIPS CPU in 1996 *(see **0714MSB.PDF**)*. The company also plans to provide an SH7000 ASIC core next year. The new parts mark the first step in this plan and meet the original goals. To become a significant PDA player, however, Hitachi must also attract software and system vendors in a market where many major players have already made commitments; a 200-MIPS processor, even in 1996, could be quite attractive. ♦

	SH7034	SH7020	SH7021	SH7604
CPU Core	SH-1	SH-1	SH-1	SH-2
MAC Unit	16-bit	16-bit	16-bit	32-bit
Divide Unit	no	no	no	yes
SDRAM Support	no	no	no	yes
On-Chip RAM	4K	1K	1K	4K cache
On-Chip ROM	64K	16K	32K	none
DMA Channels	4 chan	4 chan	4 chan	2 chan
Interrupts	8 IRQs	8 IRQs	8 IRQs	16 mux'd
Serial Ports	2 port	2 port	2 port	1 port
A/D Converter	yes	no	no	no
Counter/Timer	yes	yes	yes	yes
Pulse/Pattern Unit	yes	yes	yes	no
Clock Rate (5V)	20 MHz	20 MHz	20 MHz	28.5 MHz
Clock Rate (3.3V)	12.5 MHz	12.5 MHz	12.5 MHz	20 MHz
Dhrystone (5V)	16 MIPS	16 MIPS	16 MIPS	25 MIPS
Dhrystone (3.3V)	10 MIPS	10 MIPS	10 MIPS	20 MIPS
Power (5V)	500 mW	500 mW	500 mW	500 mW
Power (3.3V)	130 mW	130 mW	130 mW	200 mW
IC Process	0.8 µ, 2M	0.8 µ, 2M	0.8 µ, 2M	0.8 µ, 2M
Die Size	92 mm^2	59 mm^2	59 mm^2	82 mm^2
Package	120 TQFP	100 TQFP	100 TQFP	144 PQFP
Est. Mfg. Cost	$20	$13	$13	$20

Table 2. The SH70xx parts differ mainly in the amount of on-chip memory, but the 7604 implements a new feature set.

