High-End Embedded Processors Evolve in ’93

Modular Design and Shrinking Process Pack More onto Chips

by Curtis P. Feigel

Thirty-two-bit embedded microprocessors experienced a year of refinements and upgrades across a broad range of devices, with just two new architectures to show at the end. Processors that were the hot ticket for workstations just a few years ago are now available as high-end embedded devices, doubling and tripling the available processing power. Meanwhile, processors with low cost, high performance, and miserly power requirements have been introduced for PDAs, consumer electronics, and embedded systems.

In a field that was formerly dominated by a few high-end players, the end of 1993 finds established vendors consolidating their positions against numerous upstart competitors. Several manufacturers are moving toward a modular design philosophy, allowing customers to specify a single-chip system built around a processor core and customized with peripherals.

Little Parts Make Big Picture

In the realm of high-end embedded applications, Intel’s i960 series and AMD’s 29000 family continue to dominate the market, with Intel the volume leader due in large part to the i960’s design win in HP’s LaserJet 4. Behind these two juggernauts comes the MIPS architecture in various forms from various makers. It is notable that neither Intel nor AMD introduced new processor core designs in 1993, but only variations on existing ones. The one new core in the MIPS camp, the R4600, won’t be attractive for embedded applications until LSI Logic integrates some peripherals onto the chip.

In the case of the i960, new chips were delayed by the design group’s move from Oregon to Arizona. Most of the engineers did not move but were integrated into Intel’s P6 program. As a result, the company had to build a new design team, which cost it the better part of a year. AMD’s 29000 family may also have fewer engineering resources available because of the company’s efforts to build its own x86 devices.

At the not-so-high end, AMD and Intel compete for position with their 386-architecture embedded processors. Motorola’s multitude of embedded 68000-style processors dominates applications that need lower cost rather than raw performance. Motorola’s method seems to be to find a buyer with a large-volume application, build a processor with the required peripherals, and then sell the device to the merchant market too.

The past year also saw architectures migrating into the embedded market from elsewhere. Oki and Hitachi both introduced chips based on HP’s PA-RISC architecture, which, until now, has been found only in the workstation market. At the extremely high end, Digital announced a 66-MHz embedded Alpha chip.

The overlap between embedded systems and PDAs gave some processors two markets to aim for. ARM received support from its new licensee, Texas Instruments, which is pushing the architecture into automotive applications. The Hobbit processor would fit this category, too, but AT&T is not pitching it as an embedded processor.

The only completely new architectures for embedded applications came from Hitachi, which revealed its SH7000, and from NEC, which introduced the V800. Each employs a simplified RISC-like processor that allows for 16-bit instructions. The smaller instructions yield more compact code and thus require less memory. At least initially, these processors will be aimed at consumer products. Neither implementation includes memory management—virtually a requirement to run a modern general-purpose or PDA-type operating system.

Intel Notices Embedded 386 Market

In the past few years, Intel has ignored the market for a high-end embedded x86 processor, expecting designers to turn to its i960 line. Its only other offering has been the 80186, an enhanced 8086-compatible processor core with integrated system logic that made it suitable for building low-cost general-purpose or embedded systems. The ’186 has been attractive to the embedded market for a number of reasons, including development tools and hardware that were readily available and familiar to PC users. Demands of many modern embedded applications have outstripped the ’186, however, which is now relegated to the lower end of the performance spectrum.

Now Intel has come back to defend its x86 turf with three new devices based on the 386 core. The first is a static version of the 386SX that includes no integrated system logic but can run at any clock speed up to 25 MHz (although it is rated for 5 V only). The 386CX uses the same die but has SMM (system management mode), an extended 26-bit address range (to match PCMCIA’s), and can run from supplies as low as 3.0 V. The third device is the 386EX, slated to be available next year. It will add serial and parallel I/O, a timer/counter, and DRAM refresh circuitry.

In 1993, AMD announced the Elan family, based on its static 386 processor core. The first product, called the

386SC, contains logic to directly control DRAM, a keyboard, an LCD display, serial and parallel I/O devices, and even PCMCIA cards. It can run at up to 33 MHz on 3.3 V and incorporates SMM to support power-management software. Even though this device is aimed at the subnotebook market, it is also attractive for some embedded designs.

The 386SC comes from AMD's Customer-Specific Products division, which alters processors to fit applications. With this capability, AMD has the opportunity to create a whole family of embedded Elan variants by adding or subtracting functions in the 386SC.

None of these 386 variants has a competitive price/performance ratio when compared with embedded RISC microprocessors. At $39, Intel's 386EX is less expensive than AMD's $49 386SC, but a designer could get better performance than either for about the same cost by using, say, a 29000-family processor. The most compelling reason to use these devices in an embedded application is their ability to run DOS or even Windows, if that is useful for the application.

AMD 29000, Intel i960 Slug It Out

Dogged by its perennial adversary, the Intel i960, AMD's 29000 family continues to do well. Although the Intel device won the LaserJet 4 Battle of 1992, AMD garnered a large number of sockets in 1993; for example, Apple chose the 29205 processor for use in LaserWriter 310s, and Lexmark designed 29000-family processors into five laser printers carrying the IBM label.

Intel has made no major changes to the i960 series since the addition of the 'CF. That part has now migrated to a 0.8-micron CMOS process, allowing it to run at 33 MHz. The company indicates that it will introduce two new versions of the i960 in 1994. Intel estimates that the first device, code-named P100, should reach 25 Dhrystone MIPS—more than double the performance of the i960KA at about the same price. It should be available in the first half of 1994. Intel says the second processor, the P110, should reach the 100-MIPS level and will be available sometime later in 1994.

The 29000 line has been buoyed by the addition of three new processors, which began sampling in the spring of 1993. Recognizing that customers were looking for lower-cost devices with higher levels of integration, AMD introduced the 29240, 29243, and 29245. These devices integrate function blocks similar to those found in the 29200 laser-printer controller. They also benefit from core enhancements developed for the 29030 processor and include on-chip cache.

These three processors are static devices and have serial and parallel I/O as well as a built-in DRAM controller. The higher-performance devices, the '240 and '243, include DMA and MMU functions. The '245, the low-cost device, has neither. Both the '240 and '245 have a serializer/deserializer to drive an imaging engine, such as would be found in a laser printer. AMD boasts that the '243, which is aimed at communications applications, is the only microcontroller with parity generation and checking on-chip. All three devices are pin-compatible with the earlier 29200 and 29205 processors yet are twice as fast.

To this point, all 29000-family processors have been based on essentially the same core design. Perhaps this indicates that AMD's customers have not been screaming for higher performance. It should also be noted that, at the same clock speed, the single-issue AMD processor core achieves better performance than Intel's i960CA, which is superscalar. Now AMD has revealed that it will announce an even faster processor in 1994. This will be a high-end device that is both binary- and pin-compatible with current 29000-family processors. The processor core will be enhanced, but AMD has not said whether it is a next-generation redesign, a simple process shrink, or something in between.

68000 Family Leads in Modularity

Motorola has the broadest line of embedded processors, fielding 16 distinct devices built around six different processor cores—and that's not counting the 8- and 16-bit families! In the 68000 lineup alone, performance ranges from 2.5 to 29 Dhrystone MIPS.

For several years, Motorola has been using a modular design philosophy. By combining standard function blocks with various processor cores, Motorola tailors

Major Embedded Events of 1993

NEC, LSI, Sony, and HDL created processors around the R3000 core, aiming them at embedded applications *(see **0703MSB.PDF**, **0709MSB.PDF**, and **071506.PDF**)*.

AMD's 29205 embedded processor won a significant design-in as the controller in Apple's LaserWriter 310 *(see **0705MSB.PDF**)*. AMD then launched three new, upgraded versions of the device *(see **070702.PDF**)*.

Motorola reaped the rewards of modular design with a line of 68300-family processors that fit a broad range of embedded applications *(see **070603.PDF** and **0715MSB.PDF**)*.

IBM, Oki, and Hitachi began to push versions of their high-end processors into the embedded market *(see **0711MSB.PDF** and **071507.PDF**)*.

Digital followed suit by pushing a very high-end embedded chip into the market *(see **071201.PDF**)*.

After years of neglecting the need for a higher-powered 'x86 embedded processor, Intel awoke and produced three versions of its '386 for that market *(see **071405.PDF**)*. AMD was hot on Intel's heels *(see **071404.PDF**)*.

Processor Core	Device Name	Manufacturer	MMU	DRAM Controller	DMA Channels	Serial Ports	Other Features	Price
29000	29240	AMD	√	√	4	2	raster interface, ROM ctlr., multiply	$ 88
29000	29243	AMD	√	√	4	2	parity, ROM ctlr., multiply	$ 97
29000	29245	AMD	√	√	2	1	raster interface, ROM ctlr.	$ 69
R3000	VR3800	NEC						$ 34
R3000	na	HDL					(macrocell design) opt. mult./acc.	na
R3000	R3100	Sony					(internal use) mult./acc.	na
R3000	LR33120	LSI Logic					video controller, BitBLT engine	$ 70
R3000	LR33300	LSI Logic		√				$ 50
R3000	LR33310	LSI Logic		√				$ 75
R4000	R4600	IDT						
386	386SC	AMD		√	1	1	PCMCIA interface, graphics, ISA	$ 49
386	386SX	Intel					static	
386	386CX	Intel			2		64M address range, SMM	$ 27
386	386EX	Intel				3	DRAM refersh, 3 timers	$ 39
68000	68307	Motorola				2	2 timers, 8051-type bus	$ 11
CPU32	68341	Motorola			2	3	2 timers, real-time clock	$ 20
CPU32+	68349	Motorola			2	2	4K SRAM, 2 counter/timers	$ 26
CPU32+	68360	Motorola		√	16	7	serial-protocol processor, 5 timers	$ 50
PA-RISC	PA/50L	Hitachi	√				FPU, SDRAM support	$ 95*
PA-RISC	OP32/50N	Oki		√	4			$120*
21066	21068	Digital		√			FPU, PCI interface	$221
ARM7	ARM700	Plessey	√					$ 35
SH7000	SH7032	Hitachi			4	2	ROM, RAM, 5 timers, 8 A/D, PWM	
V800	V805	NEC					FP instructions	$ 28
V800	V810	NEC					FP instructions	$ 20
V800	V820	NEC		√	4	2	FP instructions, 1 timer	$ 80

Table 1. Only the SH7000 and V800 architectures are new for 1993. * Estimated mfg. cost.

chips for customers with specific target applications. Once complete, the company makes the new version available to the rest of the world. This is why there are so many devices in the 68xxx line.

Motorola divides its high-end processors into three broad product lines:

- The 680x0 devices are primarily for general-purpose computers, though the majority probably go into embedded applications.
- The 68EC0x0 devices are built without the FPU and MMU and so are lower cost, but each offers the same integer performance as its bigger sibling.
- The 683xx devices offer the highest level of integration and are typically the ones picked for new embedded applications.

This third product line can be further divided by the processor cores used. Low-end processors such as the 68306 use a 68000 core with additional simple function blocks such as serial I/O, timers, and glue logic. Mid-range devices such as the 68330 and the 68331 are built around the CPU32 core (a superset of the 68000 and similar to the 68020), so performance is approximately doubled. A further-enhanced core, called CPU32+, achieves higher performance due to its separate internal data and instruction buses. The final division of processors consists of devices that include both a 68000-family core and one of several processing elements specialized for an application such as communications or real-time control.

Motorola added several 683xx processors in 1993, among them the 68307, 68360, 68341, and 68349. The ’307 is the first device in the family to use a static 68000 core (CPU32-based devices are fully static) and incorporates a bus interface that can talk to 8051-type peripherals. The ’341 is an upgrade to the 68340 that contains extra serial I/O circuitry and a real-time clock. The ’360 QUICC (quad integrated communications controller) incorporates both a CPU32 core and a dedicated processor microcoded to handle eight different communications protocols. A special ’EN360 version is available that also handles Ethernet.

The ’349, also known as Dragon I, is part of a two-chip set designed in collaboration with General Magic. The chip set will provide a highly integrated solution for building PDAs to run that company’s Magic Cap operating system. The ’349 is the first 683xx family member to have an instruction cache.

Motorola claims it will introduce eight new processors in 1994 and 16 the year after, by which time, it says, artificial-intelligence software will be available to help the sales force recommend the right product from the lineup. The company’s timetable includes plans to introduce, by midyear, an integrated version of its 68040 processor that includes a DRAM controller.

Motorola is aggressive in maintaining its position as the customization leader. Even versions of the upcoming superscalar 68060 will be available for tailoring to customers’ needs. Because this device will be fully synthesizable, embedded customers can ask Motorola to delete from and add to the processor core in a wholesale manner, even to the point of reducing it to a single-issue machine. This technique goes well beyond allowing a system designer to specify cache sizes that make sense for a particular application.

With this level of control, Motorola may allow even more subtle changes that would retarget the ’060 squarely at the embedded market. The company suggests, for example, getting rid of such features as bit-field operations, extended-precision math, and the branch cache, and simplifying the pipeline by eliminating certain kinds of addressing. This would make a simpler, less

expensive, and possibly even faster processor. Because the 68040 was not designed with this customization in mind, it is less amenable to customer-specific designs.

Many of Motorola's current processors are available in both 5-V and 3.3-V designs. The upcoming 0.5-micron devices will be limited to a maximum of 3.3 V but will still provide TTL-compatible I/O.

ARM7: Performance in a Small Package

Shipment of Apple's Newton PDA in 1993 made the ARM6 series a volume product and raised the credibility of the ARM architecture. ARM won another major design-in when 3DO selected the ARM60 for use in its interactive video product. Reportedly, the choice was made based on the ARM device's price/performance ratio. Apple reportedly selected the ARM610 for Newton because of the processor's low power consumption.

Sharp, Texas Instruments, and Cirrus Logic all announced license agreements with ARM in 1993. Even though Sharp is currently the builder of Newtons for Apple, it has only recently achieved first silicon of the ARM610, so most of the processors in Newtons come from another ARM licensee, GEC Plessey. Sharp expects to have production volumes of the '610 in the first quarter of 1994. Cirrus Logic has plans to build a system-logic chip set for Newton devices and later combine it with the ARM core into a single chip.

TI's ARM license covers only derivative chips for application-specific products, not general-purpose CPUs. TI, as one of the world's major semiconductor vendors, has the muscle to promote the ARM in automotive applications—another potential high-volume win for ARM. VLSI, yet another licensee, has been supplying ARM silicon for more than four years. It is now developing a family of embedded microprocessor products, including the ARM650 microcontroller, an encryption engine, and a communications controller.

The ARM7 series, which was announced at this year's Microprocessor Forum, is a redesign of the ARM6 core that eliminates about 5% of the latter's transistors and compacts the rest of the processor core into an area of only 6 mm^2—close to half the original's size. Significant side effects are that the clock speed is increased 33% and both power and cost are reduced. The ARM7DM and '70DM variants include a fast integer multiplier that makes them suitable for medium-performance DSP applications.

The ARM7 architecture may be licensed as an ASIC macrocell, or purchased in silicon form from ARM licensees. TI and VLSI will include the ARM core in their libraries of standard cells and can combine the it with various peripherals and function blocks. VLSI is offering to include fuzzy-logic hardware for embedded applications. Early in 1994, Sharp will roll out product plans for combining the new ARM7 processor with memories and peripherals. Plessey is sampling the ARM700, and gives its price as $35 in 10,000-unit quantities.

MIPS Throne Has Many Contenders

While the MIPS architecture has had its problems in the desktop arena, it maintains a solid position in the embedded market. Four different companies announced seven MIPS-derived embedded controllers during 1993. In March, NEC introduced its R3000 variant for the embedded market, followed later that spring by announcements from Sony and HDL. The NEC device, called the VR3800, includes on-chip caches and clock generation and, to keep the cost down, not much else. Available in speeds from 16 to 25 MHz, the VR3800 costs from $40 to $49. NEC's R4200, with its high performance and cost of $80, would also seem to be a natural for embedded applications, although the company isn't promoting it that way. Sony's custom MIPS core will be built into that company's consumer products, but Sony has no plans to sell it on the open market.

HDL's core began as a commercial Verilog model of the MIPS R3000 processor. IDT used this model to simulate some of its R3000-family processors. The success of the model allowed HDL to alter its business strategy to become a flexible provider of customer-specific processor designs—combining the processor core with the customer's peripheral logic for production in a gate-array or standard-cell process. HDL claims to have achieved 33-MHz operation at 3 V. The chip's designers eliminated the MMU to save space, resulting in a core just 9 mm^2—about half the size of the other vendors' MIPS cores. The new core is finding its way into cable set-top boxes, multimedia add-in cards, fiber-channel interfaces, and other mostly high-volume, low-cost applications.

IDT's major announcement for 1993 was its R4600 "Orion" processor, a new processor designed by a company called QED to be code- and pin-compatible with the R4400 but at a lower cost. The R4600 is billed as both a high-performance processor aimed at Windows NT and a high-end embedded processor. IDT's embedded line includes three processor families based on the R3000 that incorporate cache on-chip but have no I/O on board. No changes occurred to this lineup in 1993, but IDT plans to follow the same path it did with its previous MIPS designs and produce an embedded R4600.

LSI Logic Customizes R3000

In the summer of 1993, LSI Logic claimed the title of the industry's fastest X-terminal controller. Announced as an upgrade of its LR33020, the LR33120 combines an R3000 core, a video controller with a Bit-BLT engine, and specialized I/O. LSI rates the device at 150,000 Xstones.

LSI also began to employ its own modular customization program. Referred to as "CoreWare," the

scheme gives designers the CW3330 (an R3000 core) and a set of standardized function blocks to assemble a system on a chip. Megacells for I/O and bus interfaces, memory controllers, graphics engines, and image compression already exist in LSI's library, and customers are free to incorporate their own application-specific logic. The company also has megacells that implement communications protocols for Fiber Channel, Ethernet, and ATM.

Using LSI's portfolio of CAE tools, customers specify their system in a hardware description language such as Verilog or VHDL, which is then run through a process of modeling, synthesis, and optimization. LSI then fabricates the device in its 0.6-micron ASIC process. From tape-out to finished product is said to take three weeks. LSI expects to shift to a 0.5-micron process in mid-1994.

CoreWare is significant because it provides flexibility of design, a high level of integration, and a short time-to-market. LSI used the method to produce the LR33300 and LR33310, two processors that will be sold in the merchant market (samples will be available in the first quarter of 1994). Like LSI's LR33000, these incorporate caches on board but have little in the way of peripherals, although they do include timers and a DRAM controller block. The company claims that, at the same clock speed, the new core is 30% faster than the old one.

New Architectures Appear

Despite the number of processors already in existence, 1993 saw several architectures introduced into the embedded market. Some were existing architectures that migrated into the embedded arena, while others were completely new.

NEC began shipping its V800 architecture, embodied in the V805, V810, and V820. The latter two chips have 32-bit-wide data and address buses, while the V805 has its data bus narrowed to 16 bits to fit in a less expensive package. The V820 includes a memory controller, a timer, and serial I/O on one chip. The architecture is notable because, although it has a large RISC-like bank of 32-bit registers, it bends RISC's rules by using both 16- and 32-bit instructions. This peculiarity stems from a desire to achieve very dense code and thus reduce cost and power consumption for small systems.

The Hitachi SH7000 also premiered in 1993. Basically a RISC machine, its simple architecture keeps its core small. Its initial implementation is aimed at consumer products. Later versions will be capable of running the protected operating systems commonly used in PDAs. It uses 16-bit instructions exclusively and includes integer multiply-accumulate instructions.

In the high-performance arena, Hitachi and Oki introduced integrated and embedded-processor versions using HP's PA-RISC architecture. IBM piqued people's interest with the possibility of a "400" line of PowerPC processors for embedded systems but made no product announcements and offered no details. Motorola will also push PowerPC as embedded processor; its deal to provide Ford with processors for automotive-control applications requires a low-cost PowerPC processor, possibly accomplished by simplifying the device's implementation and reducing its performance. Digital got into the picture by announcing its 21068 Alpha chip, a slower-clocked version of its 21066 that benchmarks at 70 Dhrystone MIPS, as an embedded processor. The '068 is the first in a family of embedded Alpha processors that will reach lower prices as new designs emerge.

Embedded Processors Become Modular

The examples of Motorola and LSI bring into focus the emerging trend toward modular integration. Processor cores and various peripherals are becoming standardized and are being used as building blocks. Simulation models of these blocks are available for designers to use in specifying single-chip solutions. Different vendors are taking different approaches with this concept. Intel's i960 remains a generic, general-purpose processor. AMD has selected just a few target applications and is customizing the 29000 for them. Motorola's engineers take on any job with sufficient volume, develop a customized version of the standard processor, and put each new variant in the catalog. Companies such as LSI Logic, VLSI, and Texas Instruments treat processors and peripherals as megacells in their ASIC libraries.

As IC manufacturing processes improve, feature sizes grow ever smaller, voltage and power are reduced, and the system itself can shrink. This trend has enabled powerful handheld devices, such as portable digital cellular phones. As the die size gets smaller for the same number of functions, the cost decreases. If the die size stays the same, the number of functions can increase, making the device easier to use, lowering the chip count, and lowering system cost. Either way, the price/performance ratio becomes more favorable.

Manufacturers will continue to look for ways to exploit new and smaller processes other than reducing die size (which often doesn't happen anyway, if the device is pad-limited). Many embedded applications don't require a high-performance processor with an MMU, floating-point unit, or large caches. These applications will gain, however, from increased integration. A side effect is that lowering the cost of adding circuitry reduces the need to fully optimize the design, so development effort and time to market are reduced as well.

As happened years ago with MIPS and SPARC, vendors of other workstation-class processors see the size of the embedded market and want in. For now the game is high volume and low cost. Some vendors may find a niche and be happy or even prosperous, but for architectures like Alpha and PA-RISC to have a major impact would require something we haven't yet seen. ♦

