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Acer Announces R4000 System Logic Chips

Alternative Designs by MIPS, DeskStation Also in Development

By Linley Gwennap

Acer has announced a system-logic chip set for PC designers using MIPS' R4000-family CPUs. The eight-chip set, called PICA, is the first of several MIPS chip sets expected to be available for the emerging Windows NT systems market. It provides a complete interface to second-level cache, main memory, and I/O for an R4000PC or R4400PC processor. It uses a new high-bandwidth bus for video and memory and connects to standard PC buses for expandability. NEC will probably be a second source for this chip set.

Two other forthcoming designs provide a "bridge" between the R4000 and standard 486 chip sets. DeskStation (Lenexa, Kansas) created such a design for its ARCStation 1 system *(see **0617MSB.PDF**)*; IDT has announced plans to market this implementation in 3Q93. MIPS itself is developing a similar bridge that it expects Toshiba and NEC to begin selling in 3Q93.

Acer believes that its chip set can be used to build a system powerful enough for Windows NT that could sell for under $4000. The MIPS and DeskStation designs, by relying on standard PC components, could be used in systems with an even lower price tag while offering better performance than 486-based PCs.

PICA Uses Four Levels of Buses

The Acer chip set uses a tiered approach to optimize the cost/bandwidth tradeoff for each device. Figure 1 (see below) shows a typical system using PICA. The processor and its external cache use the fast R4000 system bus. At the next level, high-bandwidth devices such as memory and graphics/video use a 64-bit bus to move data quickly without blocking CPU-to-cache accesses. The third tier allows a variety of I/O devices to connect using a low-cost interface. Finally, either EISA or ISA can be used for standard expansion cards.

To reduce cost, PICA works with the "PC" version of the R4000, which does not directly control a second-level cache. The CPU/Cache Controller (CCC) provides the external cache support; this is cost-effective because the R4000PC is much less expensive than the R4000SC, which includes a second-level cache controller.

The Acer design allows a second-level cache of either 128K or 256K. (Minimal systems can omit this cache entirely.) A 128K cache typically uses four 16K × 16 parts, while the larger version requires eight parts. Acer recommends using a Performance Semiconductor SRAM that is interleaved internally with two banks. Standard SRAMs can also be used but require more glue logic. The 12-bit tags are stored in two 8K × 8 SRAMs. To allow snooping in parallel with processor accesses, the design uses dual-ported tag RAMs from IDT.

Acer believes that the best performance is achieved by configuring the R4000 with 16-byte lines in its on-chip data cache and 32-byte lines in its instruction cache (because instruction references are more localized). The unified second-level cache is direct-mapped and uses 16-byte lines.

The company calls its design a write-back cache but it actually uses a write-through protocol. All writes, including misses, allocate lines in the cache and broadcast their data to the rest of the system, ensuring cache consistency. The cache has no "dirty" bits. The two FIFO chips combine to create a 16-byte queue that can buffer a single data write. Thus, the processor will not stall on a write unless it is issued before the previous write completes. The FIFO chips also provide a 32-byte queue for reads, matching the instruction cache's line size.

Cache coherency for the CPU's on-chip caches must be maintained by software (i.e., flush cache blocks before DMA). To keep the secondary cache data valid, the CCC snoops I/O transactions, removing this burden from the OS. The chip set does not support multiple processors.

In a typical design with 25-ns SRAMs, the first doubleword is returned in 4 bus cycles and the second comes 2 cycles later (i.e., a 4-2 access pattern). For maximum performance, more expensive 12-ns parts provide a 3-1 access pattern. Because the R4000 CPU runs at a multiple of the external bus speed, these cycle numbers must

be multiplied to calculate processor wait states.

The processor-bus frequency is specified at 50 MHz maximum, which allows for an R4000PC or R4400PC at 50/100 MHz (bus/CPU clock) or an R4400PC at 50/150 MHz. Since the forthcoming Orion and VRX processors both retain the R4000 system interface, Acer expects these chips will work with the PICA chip set when they become available around the end of this year.

PICA Bus Used Instead of PCI

Acer evaluated building a PCI interface but decided to develop its own bus structure instead. The company believes that the cost of interfacing to PCI, particularly as a bus master, is too high. Also, PCI does not support multithreaded I/O efficiently (see description below), and Windows NT makes heavy use of this function.

Instead of using PCI, Acer defined the 25-MHz PICA bus, which carries addresses and data multiplexed onto a single 64-bit bus, twice as wide as the current PCI. In the Acer design, only the memory and video subsystems connect to the PICA bus. I/O devices use a demultiplexed 32-bit bus that is very similar to a 486 local bus. At 25 MHz, this bus provides much more bandwidth than ISA or EISA but supports standard I/O devices for the 486. For additional expandability, any ISA or EISA bridge can be used.

Two chips connect PICA to the VL-like peripheral bus, which Acer calls the "remote" bus. The I/O Bus Controller (IBC) converts the protocols and can act as a master on either bus. The I/O Cache chip (IOC) contains a four-entry, 128-byte cache to buffer transactions in either direction. This cache has a "scatter/gather" function that takes data from multiple reads on the remote bus and performs a single burst write on the PICA bus.

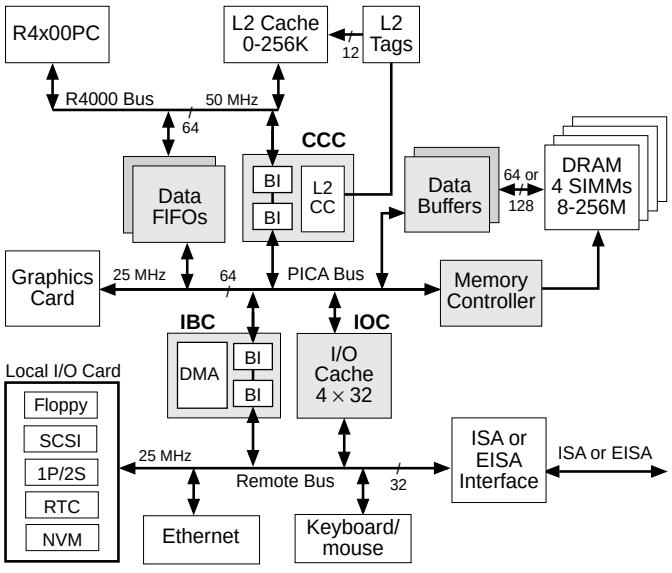

Figure 1. Acer's PICA chip set (in gray) adds a secondary cache to the R4000-family CPU while providing a high-bandwidth path to the main memory and graphics/video subsystem. Peripherals are supported on a VL-like bus with ISA (or EISA) for expandability.

Since the Acer design provides a 36-bit virtual I/O space (mapped into a 24-bit physical I/O space), the IBC has a four-entry TLB that contains both physical and virtual tags for the four entries in the I/O cache. Using its TLB, the IBC can support up to four active contexts simultaneously without flushing its cache. The TLB is updated by HAL (hardware abstraction layer) software provided by Acer. (The HAL contains hardware-specific code for Windows NT) *(see **061102.PDF**)*

High Bandwidth to Memory and Graphics

The PICA bus provides 200 MBytes per second of peak bandwidth (burst mode) to the memory and video subsystems. Three chips implement the interface to main memory: the memory controller (MC) and two data buffers. The MC provides address and control for up to 256M of DRAM. It allows for various speeds of DRAMs, page mode or normal mode, and automatically configures for the amount of memory that is installed. The MC can refresh memory without using the PICA bus ("hidden refresh") and refreshes its four banks at different times ("staggered refresh").

The MC supports a memory data width of either 64 or 128 bits. With relatively inexpensive 80-ns DRAMs, the memory can keep pace with the 25-MHz PICA bus; page-mode hits return data in a 3-1-1-1 pattern. From the viewpoint of the 50-MHz processor bus, this 32-byte read would take 14 cycles.

Acer claims that the PICA protocol is close enough to VL-Bus that current graphics chips can be connected with only a small amount of glue logic. This logic must also convert the 64-bit PICA bus to the 32-bit interface of most graphics chips. The company hopes that high-end graphics vendors will eventually add PICA to the list of buses that they directly support.

DeskStation Design Bridges to OPTi Chips

DeskStation took a different approach to building a low-cost R4000 system. Instead of designing a complete system-logic chip set, it took advantage of an existing 486 chip set by constructing a simple interface to the MIPS processor, as shown in Figure 2. The control logic translates the R4000 bus protocol into a 486 bus protocol, and drives the external cache. The buffers pass data between the CPU and the system-logic chip set.

The second-level cache is direct-mapped and uses a write-through mode. It is two-way interleaved, which allows 25-ns SRAMs to provide data at the full 50-MHz clock rate after the initial access (i.e., a 3-1 access pattern). The line size is 16 bytes, expandable to 32. There is no hardware snooping; software must maintain the consistency of all caches.

The cache size can be 128K to 1M, but since the in-

terleaving requires a 128-bit data width, a typical system with 32K × 8 parts will have a 512K cache. The tags are only 9 bits wide, which allows for a single tag RAM but limits main memory to 512 times the cache size.

The DeskStation design uses OPTi's EISAWB chip set for DRAM control and an interface to EISA. The OPTi chip set controls up to 256M of DRAM with programmable timing and page-mode access. Like the Acer memory controller, it supports hidden and staggered refresh. As in most x86 designs, however, the memory width is only 32 bits, so memory accesses will be slower than with PICA. DeskStation has not tested its design with other PC chip sets but believes that there should be no compatibility problems.

Integrated Device Technology (IDT) has licensed the DeskStation design and is developing plans to make it available to customers in 2H93 as a 120-pin ASIC for the control logic and three 120-pin buffer chips. IDT announced its intent to market these chips itself but now says it may sub-license the design to another vendor.

MIPS ODC Builds Its Own Bridge

MIPS originally attempted to jump-start the R4000PC market with its "Jazz" chip set, or ARCset *(see **060601.PDF**)*. That design, with its large and complex ASICs, proved too expensive for sub-$5000 PCs. Now, the company is developing a lower-cost R4000-to-486 protocol converter for use by its Open Design Center (ODC) customers. The result, shown in Figure 3, is quite similar to the DeskStation design. Instead of a single control chip, both bus control and data buffering are split between the two chips, which are basically identical except that the cache chip controls the secondary cache.

Unlike the DeskStation design, the MIPS cache is not interleaved, allowing for smaller sizes if desired. Without interleaving, it requires more expensive (15-ns) SRAMs to match DeskStation's performance, but it can also use slower parts if added wait states are tolerable. The MIPS design uses two tag RAMs, so tag width is not a problem. Other cache parameters are identical: direct-mapped, 16- or 32-byte cache lines with a write-through protocol and no snooping.

Since the MIPS chips can work with a variety of PC chip sets, the system designer can select one that provides the desired memory control and expansion bus (i.e., EISA or ISA) capabilities. The current design runs at 5V, but a future version will move to a 3.3V technology, making it well-suited for a portable system based on a VRX or Orion processor.

The MIPS chips will be manufactured and sold by its semiconductor partners; Toshiba and NEC are likely candidates but neither has made a firm commitment. Samples should be available in 2Q93, with production parts in 3Q93. Pricing has not yet been set, but MIPS expects it to be around $20–$30 for the two-chip set, based on the 15K-gate technology used.

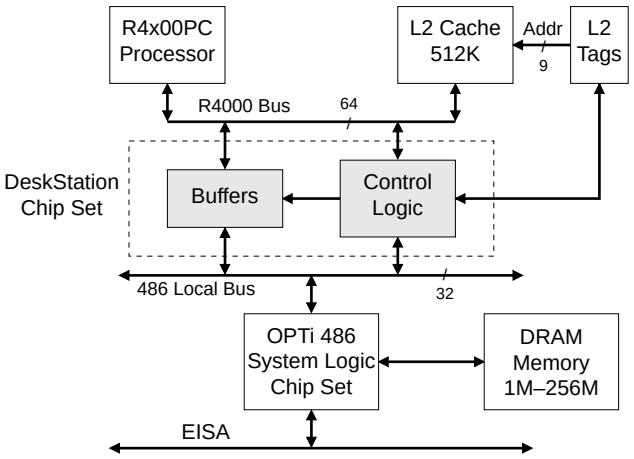

Figure 2. The DeskStation design connects an R4000-family processor to a standard 486 system logic chip set.

The ODC intends to follow the current design with VL-Bus and PCI chip sets around the end of this year. It is also supporting the Acer design.

Performance Issues

Since there are no Windows NT benchmarks available yet *(see **0705ED.PDF**)*, it is impossible to accurately evaluate the performance of any of these chip sets. Acer published a rating of 92.2 MIPS on Dhrystone 2.1 using an R4000 with the PICA chip set, which would be about the speed of a 60-MHz Pentium. Dhrystone fits in the R4000's on-chip cache, however, and thus does not stress the PICA chip set at all. SPECint92 would be a more meaningful measure, but Acer has not yet ported UNIX to its development systems (not a high priority for an NT system vendor) or ported SPEC to NT.

Thus, we must estimate performance based on the

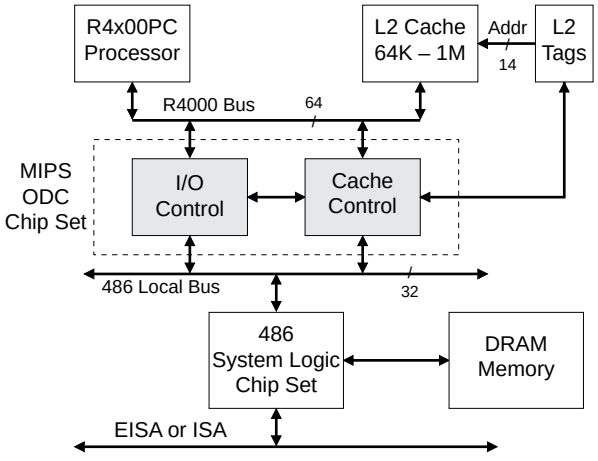

Figure 3. The MIPS chip set includes a cache controller as well as a bridge to a 486 system-logic chip set.

technical merits of the chip sets. There are two major aspects of these chip sets that impact performance: the secondary cache and the main memory. The amount of time to handle a secondary cache hit depends on the efficiency of the cache controller and the organization and speed of the SRAMs. Accesses to main memory are more complex, but we can look at the bandwidth between the main memory and the cache.

One endpoint for the comparison is an R4000PC with no external cache; these systems exist today and are rated at about 40 SPECint92. At the other extreme are R4000SC workstations with a fast external cache; these systems are rated around 60 SPECint92. The objective of the new chip sets is to improve upon the performance of a cacheless R4000PC without incurring the high costs of an R4000SC workstation.

All three of the new chips sets provide a fast secondary cache, although not nearly as fast as an R4000SC workstation. The R4000SC has the advantage of a 128-bit path to its external cache, while the R4000PC uses the 64-bit system bus. All of the R4000PC chip sets take 4 bus cycles to deliver 16 bytes, compared to 2 cycles for the R4000SC, assuming both use fast SRAMs. Typical MIPS-based PCs (as well as some workstations) will probably use less-expensive memory chips, extending the cache refill time to 6 bus cycles.

Systems using the DeskStation or MIPS chips potentially can have larger caches than PICA systems, which may offer some benefit since the multitasking Windows NT and its applications can use a lot of memory. In particular, DeskStation's preliminary measurements show DOS emulation performs much better with at least 256K–512K of cache.

The major difference between these chip sets is that the Acer design provides high performance throughout the system, whereas the others use lower-cost PC-type components. For example, the PICA memory system is quite fast; with 80-ns DRAMs, the memory can keep up with the 200-MBytes/s PICA bus, and a 32-byte read completes in just 14 processor bus cycles. This approaches the speed of a high-performance workstation design without using expensive components. The DeskStation and MIPS designs are hampered by 32-bit PC memory systems that will be nearly twice as slow.

Based on simulations, MIPS expects its chip set to perform at around 50–53 SPECint92 with an R4000PC, about 30% faster than a system without an external cache. The DeskStation design should be about the same, but MIPS projects that the Acer chip set could reach 55–58 SPECint92 with the R4000PC, nearly the speed of an R4000SC workstation.

Comparisons to Pentium Chip Sets

The PICA chip set is comparable in performance to Pentium chip sets. For example, Intel's Pentium PCIset *(see **070403.PDF**)* provides a 3-1-1-1 secondary cache access at 66 MHz with 10-ns synchronous SRAMs, while the Acer design offers a 3-1-1-1 access at 50-MHz with 12-ns standard SRAMs. With standard 15-ns parts, the PCIset access is 3-2-2-2; the PICA chip set has a 4-2-2-2 access with less-expensive 25-ns parts.

Acer's memory design is much faster than typical 486 memory systems and even edges out the Pentium chip sets. The 64-bit PICA bus is the same width as Pentium's bus, and the Acer memory system pumps out data at 25 MHz with 80-ns DRAMs. The Intel chip set requires 70-ns parts and can only deliver data at about 16 MHz, one-fourth of the Pentium clock speed.

Acer places the graphics system on the PICA bus, which has nearly twice the bandwidth of the 32-bit PCI implementation used in the Intel PCIset. PCI has more than enough bandwidth for most graphics applications; PICA might have an advantage if the CPU were transferring full-motion video from a CD-ROM to the display, for example.

PICA connects to other peripherals using a 486-style local bus. Acer believes that it is more cost-effective to connect to this bus than to PCI. Since the number of peripherals available for either of these two buses is currently small, it remains to be seen if this belief is correct.

Both the MIPS and DeskStation designs offer cache performance comparable to the Pentium chip sets. Their large secondary caches help to offset the impact of the slower 486 memory system, but performance suffers somewhat. Peripherals typically attach to the EISA or ISA buses.

MIPS Has Advantage Over Pentium

The Acer chip set, combined with an R4000PC at 50/100 MHz, should have similar SPECint92 performance to a 66-MHz Pentium system with Intel's PCIset. Intel's chip set costs $84 with an ISA interface and does not require external tag RAMs; the PICA chips cost $139 plus an extra $18 or so for the tag RAMs and $11 for the ISA interface. On the other hand, the Intel chip set uses more expensive SRAM and DRAM to achieve the same performance as the Acer design. There are too many variables for a complete analysis, but it appears that the system cost (excluding the CPU) should be comparable for equivalent configurations using the two chip sets. The R4000PC, however, will be less expensive and more plentiful than Pentium for at least the rest of 1993.

Performance with an R4400PC at 50/150 MHz should be significantly faster than a 66-MHz Pentium, and these two CPUs should be comparably priced. Thus, MIPS-based systems could beat Pentium in both absolute performance and in price/performance for the Windows NT market, assuming system vendors use a similar pricing model for both types of products.

By relying on its own bus for graphics rather than

PCI, Acer must add the cost needed to interface current graphics chips to its PICA bus. This cost could be eliminated if graphics vendors support PICA, but at best it seems that PICA will be far down on the priority list.

Another drawback of the PICA chip set is the concern for a level playing field; the chip set is being sold by a company that will also be the largest competitor of any system vendor who buys it. Acer is finalizing an agreement that allows NEC, which currently builds the PICA chips for Acer, to openly market the chip set.

Both the DeskStation and MIPS designs should provide comparable performance to the Acer chip set on cache-intensive applications, but the graphics, memory, and I/O systems are inferior to either PICA or PCI. Even so, R4000PC systems with these chips should be faster than any 486 boxes, including the expected "DX3" chips from Intel.

Without a product announcement, it is difficult to compare the price of the DeskStation design to that of actual products, but the combined price of its bridge logic and the OPTi chip set should be lower than PICA's $139 price tag. The sum of the $20–$30 estimated cost of the MIPS chip set and $25–$50 for a typical ISA chip set is much less than Acer's price. Overall system cost using the bridge chip sets will be lower due to the lower-performance system components; system prices could be comparable to current high-end 486 products with similar amounts of memory and disk space.

The combination of three chip sets from multiple vendors should make it easier for system vendors to design PCs using MIPS processors by reducing both the overall system cost and the upfront design effort; the Open Design Center is supplying design kits for $5000 *(see **0703MSB.PDF**)*. Vendors with a more advanced design capability can use these chip sets for a variety of price/performance points, allowing them to differentiate their products. The expected high price and short supply of Pentium chips may also encourage second- and third-tier system makers to use the R4000.

DEC is lagging MIPS in establishing its architecture as a low-cost system alternative. Digital is positioning Alpha as the highest-performance alternative for Windows NT, and its performance keeps going up *(see **0705MSB.PDF**)*. So far, however, there are no system-logic chip sets available for the Alpha processor. The Low-Cost Alpha chip will include a cache controller, DRAM controller, and PCI interface on the chip, virtually eliminating the need for a chip set, but it is not due until late this year. By that time, MIPS-based PCs using a variety of chip sets will be available from multiple vendors.

Even with a number of system vendors, the nascent NT-on-MIPS market may not be big enough to profitably support three chip sets. Both IDT and MIPS view their designs as ways to generate more processor sales and so may be willing to accept lower profits than on other products. With all of the pieces in place for systems with better price/performance than Pentium products, MIPS and its partners could grab a significant chunk of the Windows NT market from Intel. ♦

Price and Availability

The PICA chip set includes one CCC (M6101), two data FIFOs (M6103), one MC (M6105), two data buffers (M6107), one IBC (M6109), and one IOC (M6111). All chips are packaged in PQFPs; the M6101 package has 176 pins; the M6103, 120 pins; the M6105, 136 pins; the M6107, 144 pins; the M6109, 208 pins; and the M6111 has 160 pins.

The eight-chip set is now sampling at $199. In July, the price drops to $149 in quantities of 5000. Prices include a $10 license fee for binary ROM and HAL code. Acer America, 2641 Orchard Parkway, San Jose, CA 95134; 408/432-6200 ext. 4072, fax 408/435-8517.

IDT is developing plans to make the DeskStation design available in 2H93 as a 120-pin control ASIC and three 120-pin buffer chips but has not announced a product or pricing. Contact Integrated Device Technology at 2975 Stender Way, PO Box 58015, Santa Clara, CA 95052; 408/492-8623, fax 408/492-8674.

Toshiba expects to market the MIPS chip set but has not announced the product. NEC may also sell the chip set. MIPS expects the chips to sample in 2Q93 and reach production in 3Q93. Pricing is not determined, but should be about $20–$30 for the two-chip set. Contact Toshiba America at 9775 Toledo Way, PO Box 19785, Irvine, CA 92718; 714-455-2227.

