Intel Provides PCI Chip Set for Pentium

New PCI-to-EISA Bridge Also Works with 486 Chip Set

By Linley Gwennap

To allow system vendors to take full advantage of the performance of Pentium, Intel has announced its 82430 PCIset to interface its new processor to peripherals on the PCI and EISA (or ISA) buses. The chip set also provides interfaces to system memory and second-level cache.

From a functional standpoint, the new chip set is very similar to the 82420 chip set announced for 486 systems last November *(see **061602.PDF**)*. The old CDC (Cache/DRAM Controller) and DPU (Data Path Unit) chips have been redesigned to connect to the Pentium bus and are now called the PCMC (PCI/Cache/Memory Controller) and LBX (Local Bus Accelerator) respectively. Because of the wider Pentium bus, the LBX is sliced into two chips to reduce pin count.

The SIO (System I/O) chip from the '420 chip set provides a bridge from PCI to ISA. Two new chips, the PCEB (PCI-to-EISA Bridge) and ESC (EISA System Controller) connect PCI to EISA. Figure 1 shows the complete 82430 chip set in the EISA configuration.

Integrated Cache Tags

One major improvement over the previous '420 design is that the new chip set incorporates cache tag memory in the PCMC. This means that external SRAMs are needed for data storage only. Although this reduces the number of costly SRAMs needed, it does constrain the cache configuration somewhat. The PCMC includes 4096 tag entries, each of which can map a single cache line of either 64 or 128 bytes. Thus, the second-level cache (if implemented) must be either 256K or 512K in size.

These long cache lines are broken into 32-byte blocks. When a new line is allocated, only the needed block is read from memory. Additional blocks in the line are filled only as needed. This strategy matches the block size to the line size of Pentium's internal cache and allows a smaller number of tags to handle a larger amount of cache memory.

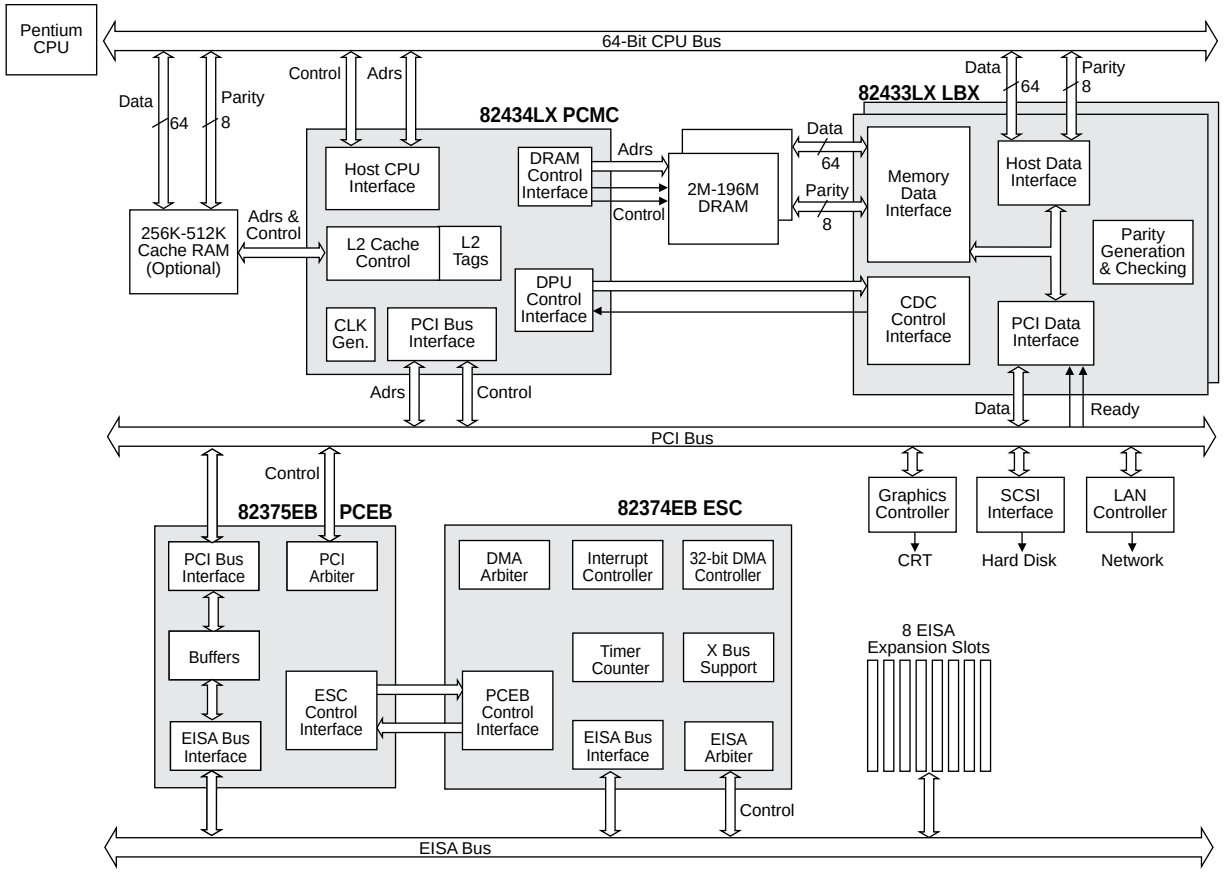

Figure 1. The 82430 chip set provides cache and memory control for a Pentium processor. It also connects to a PCI bus for high-speed peripherals and to an EISA bus (shown here) or ISA bus for standard peripherals.

82496 MP Cache Controller

For multiprocessor Pentium systems, Intel has taken its 82495DX cache control chip (see µPR 6/26/91, p. 8), originally designing for the 486, and slightly modified it for Pentium, naming it the 82496. The 82490 cache RAM was requalified at 66 MHz and is now the 82491 Pentium cache RAM. A Pentium design uses twice as many 82491 chips as a 486 design to provide a 64-bit data path. The new chips provide zero wait states (1-1-1-1 accesses) at up to 66 MHz.

The 82496 uses a 280-pin ceramic PGA and is priced at $160 in quantities of 1000. The 82491 SRAM uses an 84-pin PQFP and is priced at $36 in quantities of 1000. For more information, contact your local Intel sales office.

Price and Availability

The ISA 82430 PCIset, consisting of one PCMC (82434LX), two LBX chips (82433LX), and one SIO (82378IB) is priced at $84 in quantities of 1000. The EISA 82430 PCIset, consisting of one PCMC, two LBX chips, one PCEB (82375EB), and one ESC (82374EB), is priced at $108 in quantities of 1000. All of the chips are currently sampling with production quantities available in 2Q93.

The PCMC is in a 208-pin PQFP package. The LBX uses a 160-pin PQFP and the SIO uses a 208-pin PQFP. The PCEB and ESC are packaged in 208-pin PQFPs. The PCEB and ESC can also be used with the 82420 chip set for EISA systems; the EISA 82420 chip set is priced at $75 in quantities of 10,000.

For more information contact your local Intel sales office or request packet #HP-61 from the Intel Literature Center, PO Box 7641, Mt. Prospect, IL 60056; 800/548-4725.

The PCMC does support prefetching for graphics frame-buffer accesses. When it reads a line from the frame buffer, it automatically requests the next sequential line to try to anticipate the processor's next request. The location and size of the frame buffer are configurable by writing to PCMC registers.

The second-level cache is direct mapped. Data is always returned to the CPU with the "critical" doubleword first. The cache controller supports write-back or write-through modes, selectable at startup. In write-back mode, the PCMC snoops all PCI transactions to maintain the validity of the cache data. Like the '420 chip set, the new chip set does not support multiple processors on the PCI bus.

With the processor running at up to 66 MHz, accesses to the second-level cache take multiple cycles. With standard 15-ns SRAMs, the PCMC reads data using a 3-2-2-2 access pattern: the first 64-bit access takes 3 cycles and the next three accesses take 2 cycles. With 100-MHz burst-mode (synchronous) SRAMs, data is returned in a 3-1-1-1 pattern, with subsequent cache hits within the same SRAM row at 1-1-1-1. Intel believes the synchronous SRAMs will provide about 5% better performance than standard parts.

The smaller cache typically uses eight 32K × 8 SRAMs, while the larger cache requires four 64K × 16 parts. The PCMC also supports byte parity for the second-level cache; to take advantage of this feature, either ×9 or ×18 parts are needed. The addition of two address latch chips (for address pipelining) completes the cache implementation.

LBX Provides 64-Bit Memory Interface

The memory and PCI interfaces are very similar to the '420 chip set except that they are optimized for 64-bit data and faster clocks. The PCMC provides address and control signals for 2M to 192M of memory. Although the '420 interleaves two 32-bit banks of memory, the '430 provides a single 64-bit bank. The chip set supports 1M, 4M, or 16M SIMMs in 60-ns or 70-ns speed grades. With the faster SIMMs, burst reads use a 6-3-3-3 pattern. For the 70-ns parts, the pattern is 7-4-4-4.

Two LBX chips form a complete 64-bit data switch, routing data between the DRAM memory, CPU bus, and PCI. The PCI data bus is only 32 bits and operates at one-half of the CPU clock frequency, so the LBX chips buffer data transfers to PCI. Since PCI supports burst transactions, the chips also "gather" writes to sequential addresses and issue them in a single burst. Using this mode, data can be written to graphics or other PCI devices at the peak bus rate of 132 Mbytes per second. (These features are also provided in the '420 DPU chip.)

Support for 6 PCI and 8 EISA Masters

The EISA bus is handled by the PCEB and ESC chips. The PCEB also includes the PCI arbiter, which can handle six PCI masters (including the EISA bridge and the PCMC), two more than the SIO chip. The PCEB provides address and data connections to EISA and includes several sets of data buffers to improve performance. It supports burst transfers on both PCI and EISA buses.

The ESC contains the EISA controller, which supports up to eight EISA masters without external logic. The ESC also contains a DMA controller, X-Bus support, timers, interrupts, and other features similar to the SIO. The EISA bus is clocked at 1/3 or 1/4 of the PCI bus, up to a maximum of 8.33 MHz.

A New Level of Performance

Much of the system must be redesigned to take full advantage of Pentium's performance. Although the '430 chip set itself is reasonably priced, 10-ns synchronous SRAMs and fast PCI devices are much more expensive

than standard 486 system components. Pentium systems taking maximum advantage of this PCI chip set will be quite expensive, probably over $5,000. Cost can be reduced by using an asynchronous cache or even no cache, but this will reduce performance.

Because the new chip set has just started to sample, the very first Pentium systems will not take advantage of it. These products will either use the 82496 cache controller (see sidebar above) or proprietary ASICs combined with 486 chip sets. The 82430 will appear in a second wave of Pentium systems this fall. The 82496 will continue to be used in multiprocessor and other top-of-the line systems, since its zero-wait-state design provides 5%–10% more performance than the PCIset.

Several other vendors are also planning to offer Pentium chip sets, including VLSI Technology, OPTi, and SiS. Some of these designs will provide a direct interface to EISA, lowering system cost, or to VL-Bus. There will also be other PCI chip sets. It remains to be seen how the Intel solution will stack up against these competitors.♦

