EISA Chip Sets Emerge for High-End PC Systems

Industry Heavyweights Offer Desktop, Server Alternatives

By Mark Thorson

For the first year and a half after its public release in 1989, the EISA bus for high-end PC-compatible systems was supported by only one vendor of system logic components—Intel. The original members of the EISA consortium agreed to base the first generation of products on Intel's 82350 chip set to ensure a high degree of hardware compatibility.

Today, system designers have several alternatives to the Intel chip set. OPTi was the first to announce a competing chip set in mid-1991, followed shortly by Texas Instruments and Symphony later that year. These were joined in mid-1992 by Silicon Integrated Systems (SiS) and ETEQ. In this article, we compare all the currently available EISA chip sets.

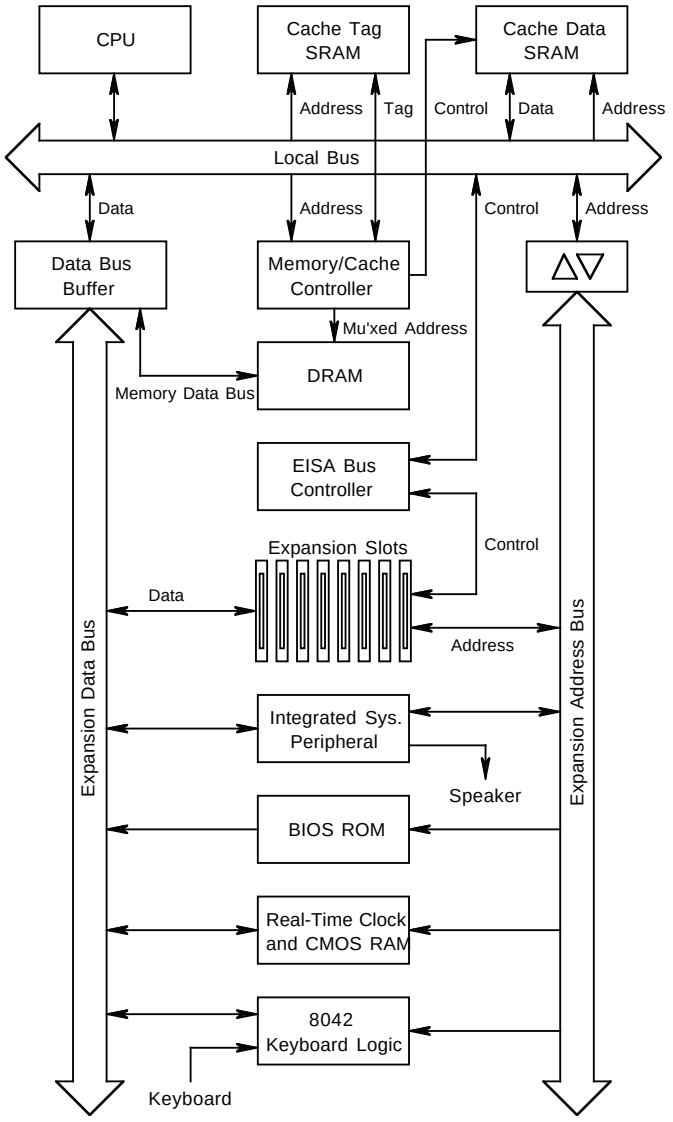

Figure 1. Generic EISA system block diagram.

EISA Background

The EISA bus emerged largely in response to IBM's introduction of Micro Channel, an expansion bus designed to replace the low-performance AT (ISA) bus. A consortium of system vendors led by Compaq developed EISA as an alternative to Micro Channel for next-generation PC systems. The features of the EISA bus—such as support for automatic system configuration, slot-specific address space, and burst data transfers—closely follow the features of Micro Channel.

The Micro Channel bus, with both 16- and 32-bit versions, was designed to replace the AT bus across the whole range of PC systems (although even IBM continues to use the AT bus in some low-end systems). EISA is intended to occupy the high end while co-existing peacefully with the AT bus for low-end to mid-range systems.

Unlike Micro Channel, EISA is upward compatible with the AT bus. The EISA edge connector has two sets of contacts spaced vertically. An AT card sits halfway down in the slot, and mates only with the upper set of contacts. An EISA card has longer tabs that reach deeper into the connector and mate with both sets of contacts.

Native EISA cycles use a synchronous protocol that is quite unlike the AT signaling mechanism. To allow interoperability of AT and EISA cards, the EISA bus controller on the system board must be able to translate between all types of AT and EISA cycles, including translations between cycles of different data size. The AT bus allows both 8- and 16-bit devices; native EISA devices can be 16- or 32-bit. Supporting the vast number of possible cycle translations seems to have been a factor in the long delay between the introduction of the EISA bus and the appearance of competing vendors for EISA chip sets.

Both EISA and Micro Channel get most of their bandwidth from increased data width and more efficient protocols, rather than higher speed. The fastest AT bus cycles consume two periods of the 8-MHz bus clock for a 16-bit transfer. EISA and Micro Channel are only marginally faster, with bus clocks of 8.33 and 10 MHz respectively. However, both EISA and Micro Channel allow burst transfers at a peak rate of one transfer per clock, in which the transfer can be 32-bit (EISA) or 64-bit (Micro Channel).

EISA Chip Sets

Table 1 compares the technical merits of EISA chip

Vendor	Chip Set Name	CPU Type	Clock Frequencies (MHz)	Cache Size	Cache Type	DRAM Size	DRAM Bank Depths	Number of Slots (Total)/Number of Slots (Bus Master)
ETEQ	ET2000	386DX/486	16–50	32K–512K	copyback	1M–256M	256K/1M/4M/16M	8/6
Intel	82350	386DX/486	25–33	n.a.	n.a.	n.a.	n.a.	n.a.
Intel	82350DT	386DX/486	25–33	n.a.	n.a.	256M	64K/256K/1M/4M	n.a.
OPTI	EISA 486WB	386DX/486	33–50	64K-512K	copyback	4M–256M	1M/4M/16M	8/6
OPTI	EISA 486AWB	486	16–50	64K-1M	(see text)	2M–128M	512K/1M/2M/4M/8M	8/6
OPTI	EISA 486LC	486	16–50	64K–1M	writethrough/ copyback	4M–256M	1M/4M/16M	8/6
SiS	EISA 486	486	25–50	64K-512K	writethrough/ copyback	1M–256M	256K/512K/1M/ 2M/4M/16M	8/6
Symphony	SL82C470	486	25–50	64K-1M	copyback	1M–256M	256K/1M/4M/16M	8/6
TI	TACT84500	386DX/486	20–33	n.a.	n.a.	1M–256M	256K/1M/4M/16M	8/8

Table 1. Comparison of EISA chip sets (n.a. = not applicable).

sets currently available. Note that some EISA chip sets can be used in several configurations with varying number of chips.

Figure 1 is a generic block diagram for a typical EISA chip set partitioning. The high-end chip sets from Intel and Texas Instruments don't include a cache controller, because it is expected that a standalone cache controller such as those from Intel, Austek, MetaDesign, Mosel, or IDT will be used. Mid-range desktop chip sets include a simple direct-mapped cache controller integrated with the DRAM controller, using external tag and data SRAMs. A proprietary buffer chip is commonly used in the data path, to accommodate packing and unpacking data for the many translation cycles between native AT and EISA bus cycles of different size. Usually, the EISA bus controller and EISA peripherals (DMA, interrupts, timers, etc.) are broken out as separate chips, however, the trend is toward more integrated solutions.

Because EISA machines generally occupy the high end of the market, obvious important factors in selecting an EISA chip set are performance (as represented by clock speed) and memory configuration (number of DRAM banks, DRAM bank depth, etc.). A less obvious selection parameter is number of slots, which is especially important in the high-end server machines that stand to benefit most from EISA's greater bus bandwidth.

Although EISA allows a maximum of 15 slots, some chip sets implement a smaller number because of pin limitations. An EISA slot has three slot-specific signals for bus masters (or one signal for slave-only slots), so bus-master support for a 15-slot system requires the bus interface to have 45 signal lines in addition to the 140 signals shared by all slots. Micro Channel is worse in this regard, because it requires each slot to be supported by four slot-specific signals (required for both masters and slaves). In the table, two numbers for slot count are shown, the first for the total number of slots that are supported and the second for the number of slots with bus-master capability. No limitation is shown for Intel's chip sets because external logic is used to handle the slot-specific signals.

Intel offers both the 82350 and 82350DT. The original 82350 lacks controllers for cache or DRAM. In mid-1991, Intel introduced the second-generation 82350DT chip set (see µPR 5/1/91, p. 15), which includes a high-performance DRAM controller and hooks for adding a discrete cache controller.

Despite the introduction of the updated chip set, demand remains strong for the original 82350. System designers seeking product differentiation at the high end of the performance spectrum often implement their own cache and DRAM solutions using proprietary logic, while using the Intel chip set to insure compliance with the EISA standard for the expansion bus.

An 82350 configuration includes the 82357 peripheral chip, 82358DT EISA bus controller, and 82351 local I/O controller (i.e., integrated random logic chip, principally for decoding on-board I/O devices). Intel also offers the 82352 buffer chip, which has strap-selectable modes allowing it to be used as either an address or data buffer. Typically, two 82352s would be used per system; alternatively, TTL or proprietary buffers can be used in place of the 82352.

The 82350DT is an upward-compatible superset of the 82350, which adds support for posted memory writes and compatibility with a new memory controller, the 82359. (The 82350 chip set doesn't have a memory controller.) A new data buffer chip, the 82353, provides buffering, steering, and parity logic between a 32-bit host bus, a 32-bit EISA bus, and a memory bus that can be as wide as 128 bits.

Having a wide memory bus is essentially equivalent to allowing two- or four-way interleaving among DRAM banks, but the memory cycles to each bank occur simultaneously rather than being staggered. Each buffer chip is a slice with six ports, in which each port has 16 data bits plus parity. In a typical system, two 82353 buffers are used for the CPU/DRAM/EISA bus paths, and one 82352 is used for buffering addresses issued to the EISA bus by the DMA controller in the 82357.

Texas Instruments offers its TACT84500 chip set, which has high-end features like the 82350DT but at a

Price & Availability

All of the chip sets mentioned in this article are in volume production. Most vendors were unwilling to quite prices for publication. Most vendors' volume pricing appears to be in the $50–60 range for a high-end chip set, or $35–50 for a low-end to mid-range chip set.

Intel, P.O. Box 58119, Santa Clara, CA 95052-8119; 408/765-8080, fax 916/351-5033.

Texas Instruments, P.O. Box 809066, Dallas, TX 75380-9066; 800/336-5236.

ETEQ Microsystems, 1900 McCarthy Blvd., Suite 110, Milpitas, CA 95035; 408/432-8147, fax 408/432-8146.

OPTi, 2525 Walsh Avenue, Santa Clara, CA 95051; 408/980-8178, fax 408/980-8860.

Silicon Integrated Systems, 240 North Wolfe Road, Sunnyvale, CA 94086; 408/735-1362, fax 408/735-7217.

Symphony Laboratories is located at 2620 Augustine Drive, Suite 250, Santa Clara, CA, 95054; 408/986-1701, fax 408/986-1771.

higher level of integration. Both chip sets have a similar system partitioning, in which there is an EISA bus controller (TACT84543), EISA-compatible peripheral chip (TACT84544), data buffer (TACT84541), and memory controller (TACT84542). A single data buffer chip with its three 32-bit ports (plus parity) is sufficient for systems with 32-bit memory; two data buffers can be paired to support a 64-bit memory bus.

OPTi offers three chip sets: its original EISA 486WB and two derivative products, the high-integration EISA 486LC and the high-performance EISA 486AWB. The EISA 486WB is partitioned like TI's chip set into the 82C681 bus controller, 82C686 peripheral chip, 82C687 data buffer, and 82C682 memory controller. Unlike the Intel and TI chip sets, the EISA 486WB includes a direct-mapped, write-back cache controller for use with external data and tag SRAMs.

The EISA 486AWB chip set includes OPTi's original bus controller and peripheral chip but replaces the memory controller and data buffer chips with upgraded designs. The suffix "AWB" refers to "adaptive write-back," a caching strategy in which write hits are writethrough to DRAM if the cycle would be a DRAM page hit, or they are writeback (i.e., the affected cache line becomes or remains dirty) if a new row address would need to be strobed in.

OPTi's EISA 486LC is a two-chip set that combines the EISA bus controller and peripheral chips into a single part. OPTi sees low cost as the main advantage of this chip set.

Symphony Laboratories offers the Mozart SL82C470, a three-chip set consisting of the SL82C472 bus controller, SL82C473 DMA controller, and SL82C471 memory controller. The memory controller supports a direct-mapped, writeback cache based on external tag and data SRAMs. The system partitioning is a little different from other EISA chip sets, because part of the peripheral set (timers and interrupt controllers) and the EISA data bus drivers are resident on the bus controller chip. Although it has only three chips, this chip set requires very little glue logic.

Silicon Integrated Systems offers a six-chip set, the SiS/EISA 486, consisting of its SiS85C420 bus controller, SiS85C406 peripheral chip, SiS85C411 memory controller, SiS85C431 data buffer, and SiS85C405 address buffer (two devices required). The memory controller supports a direct-mapped, writethrough cache based on external tag and data SRAMs.

ETEQ Microsystems offers a four-chip set, the ET2000, consisting of the ET2001 bus controller, ET2002 data buffer, ET2003 peripheral chip, and ET2004 cache/memory controller. The memory controller supports a direct-mapped, copyback cache based on external tag and data SRAMs.

Conclusions

When the Micro Channel bus and the OS/2 operating system first appeared, they threatened to render an entire generation of PC hardware obsolete. New buyers of computers—aware of the rapid depreciation of "orphan" computers—were faced with a generational break in IBM-based technology. In its early years, the existence of EISA served to blunt IBM's offensive against the PC-clone industry by offering the retail PC customer an upward growth path to next-generation technology.

EISA systems have been very successful in high-end desktop and server markets. Although Micro Channel continues to be promoted by IBM, few vendors of chip sets or systems have followed IBM's lead. Recent Micro Channel chip sets are available only from Toshiba, using designs developed by Micral's U.S. R&D center.

VLSI Technology introduced a Micro Channel chip set in 1992 using parts designed and fabricated by IBM, but active marketing of that chip set ceased a few months after it began. Research Machines—a U.K. company—also attempted to launch a chip set in 1992, and similarly withdrew.

Whether EISA or Micro Channel will play an important role in next-generation technology can be questioned. It is not clear that expansion slots will be as important in the future as they have been in the past. Some functions that traditionally would reside on expansion cards, such as floppy disk and SCSI controllers, have become common enough to include in standard system configurations.

Emerging on-board buses—e.g., VESA's VL-Bus and Intel's PCI bus *(see **060902.PDF**)*—are better solu-

tions where expansion options for high-bandwidth peripherals such as video controllers need to be offered. For low-bandwidth I/O, such as fax modems, the AT bus is adequate. In the near term, the EISA bus is most suited for niches that require high bandwidth to support multiple disk drives—principally file servers.

As the technology matures, the pricing difference between AT and EISA chip sets will shrink. Within the next few years, low-end to mid-range EISA chip sets such as OPTi's EISA 486LC could largely supplant existing AT-compatible chip sets. System vendors may still prefer to maintain separate EISA and AT product lines, however, because profit margins are highest on EISA systems. ♦

