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1992 in Review: The Top RISC Processors

Alpha Debuts at Number One while SuperSPARC Misses the Mark

By Linley Gwennap

The past year has been another busy one in the microprocessor business. Two new companies entered the merchant microprocessor business, one with a little Hobbit and the other with a big Alpha. DEC's new entry raised the bar by doubling performance and tripling clock frequency from last year's leader. Sun and MIPS finally updated their 1989 designs with new products. There were also a few products that fizzled. And, of course, the action in the x86 market has been fast and furious, but that story will be covered in our next issue. Without further ado, we present our very own RISC Microprocessor Awards (the "RISCies").

World's Fastest Microprocessor (shipping)—DECchip 21064. Digital's first-ever RISC chip is the highest-performance microprocessor shipping today. The 182-MHz version of the 21064, rated at 96.6 SPECint92 and 182.1 SPECfp92, tops the list in both of these categories, as shown below in Figures 1 and 2. A 200-MHz version should ship in 1Q93. Perhaps not coincidentally, the chip also takes the award for highest processor clock frequency and uses a very advanced IC process, with half-micron gates and a gate oxide thickness of just 105 Å.

Digital made a big splash by offering a 150-MHz 21064 on the merchant CPU market, but the only way to get chips faster than that is to buy them in servers costing $100,000 and up. Availability is limited because the yield at the higher frequencies is very low, leaving the door open for…

World's Fastest Microprocessor (shipping in volume)—PA7100. Hewlett-Packard's first single-chip processor edges out the 150-MHz 21064 for this title. (Although the 99-MHz version will not be shipping in systems until next quarter, the 96-MHz part is available today with only slightly lower ratings.) Interestingly, the PA7100 achieves this lofty performance without many of the tactics used in the 21064; the HP chip is not superpipelined, has a very limited superscalar capability (only one integer and one floating-point instruction per cycle) and uses a relatively unsophisticated IC process.

HP's insistence on keeping the primary cache off chip keeps it from playing with the high-frequency end of the yield curve. While the Alpha processor can adjust the external cache timing independent of the internal clock rate, the PA7100 requires single-cycle access to the external cache. At 99 MHz, this requires leading-edge 9-ns SRAMs. Although some small number of PA7100 chips could certainly run at much higher frequencies, there are no SRAMs available that could economically support them.

HP took some steps toward opening its architecture by forming a PA-RISC consortium called PRO and licensing test suites from 88open. The company is even making the PA7100 available to PRO members as part of a module that includes the CPU and cache. HP will not discuss pricing or general availability of these modules; the company is not ready to follow the fully-open path that DEC is blazing. In the meantime, Hitachi and Samsung have had PA-RISC licenses for three years but neither company has yet made any shipments, or even announcements, of their own PA-RISC designs.

Closest to Target—R4000. Unlike some other vendors, MIPS delivered what it said it would: a 100-MHz microprocessor. The early word from Silicon Graphics (SGI) was that its R4000 system would come in at 70 SPECmark89 (back when that was an important benchmark). When SGI finally published the actual measurements, the rating was 70.03. This award really goes to the compiler team that must have worked nights and weekends coming up with a list of compiler options as long as my arm—a different set for each of the 10 SPECmark89 programs—in order to reach that magic number.

It's been an exciting year for MIPS. When the R4000 shipped in March, it was the fastest integer processor on the market (unfortunately, it comes with a toy floating-point unit). But the effort required to finish the R4000, combined with an ill-advised foray into the systems business, sent MIPS' financial results into a tail-

spin. Silicon Graphics saved the company by buying it, but many thought they overpaid. The ACE initiative, a key part of MIPS strategy, was pronounced dead when Compaq announced it was reneging on plans to build MIPS-based PCs. DEC dumped MIPS in favor of Alpha, and other MIPS-based system vendors began bailing out.

At the end of the year, however, MIPS and SGI have successfully combined their processor plans, and the R4400 is on the way. Other than DEC, all of MIPS' top customers (SGI, Sony, NEC, Pyramid, Tandem, and CDC) have decided to stay put. Although no one talks much about ACE anymore, Microsoft has continued its support of MIPS, and R4000-based systems were prominently displayed at the Windows NT developers conference. MIPS has survived a bad year, but may lose its spot as the number two choice for RISC systems until NT-on-MIPS takes off…if it ever does.

Wide of the Mark—SuperSPARC. An arrow slashes through the air, seeking the blood-red bull's-eye at the far end of the field. THUD! The archer grimaces as the shot hits the white outer ring. This scene is not likely to appear in Sun's next commercial, but it describes the saga of SuperSPARC. Early this year, Sun spokespeople assured the press that 50-MHz chips were imminent, with 65-MHz chips available by the end of 1992 and 80-MHz chips in the future. Sun had to use 33-MHz chips to fill some early orders, and it is now shipping 36-MHz systems. Texas Instruments, Sun's partner and foundry for the design, claims to be shipping 40-MHz chips "in volume," but Sun says it will not ship significant quantities of systems at that frequency until March.

As a result, among the Big Five RISCs, the 36-MHz SuperSPARC is dead last in performance for both integer and floating-point applications (see Figures 1 and 2). Sun, which used to tout its performance, now superciliously claims (a) performance isn't important without enough software applications, and (b) desktop multiprocessing provides superior performance. It remains to be seen how well these MP systems perform on real applications, since the requisite version of Solaris has just begun shipping.

TI's pricing policy for the chip is also questionable. After announcing a low-ball $400 price for 33-MHz parts, the company now quotes $1900 for 40-MHz chips as an "average price for 1993," delivering a kick in the pants to SPARCstation-clone vendors.

SuperSPARC takes the awards for most transistors, biggest on-chip caches, biggest single die, and first major microprocessor to use BiCMOS technology (see Table 1). The chip's unique cascaded ALUs allow it to process two integer instructions per cycle even if one depends on the result of the other. These superlatives are impressive, but they also point out the problems facing Sun and TI in increasing the clock rate. The size and complexity of the chip, and the amount of work that must be done on each clock cycle, make it difficult to speed up the clock. Timing analysis for the huge design appears to have been superseded by the trial-and-error method. These problems open the door for upcoming SPARC chips from Cypress and others to try to make SuperSPARC superfluous.

Most Aptly Named—hyperSPARC. Speaking of Cypress, it continues to chase the SPARC bandwagon with its latest effort, previously known as Pinnacle. According to the company, the new hyperSPARC will be faster than SuperSPARC, competitively priced, and available real soon now. Cypress is not the first company to put "hype" in the processor name (anyone remember Hyperstone?) but it has followed through with plenty of hype in the publicity campaign.

Biggest Little Microprocessor—microSPARC. TI's junior SPARC chip allows Sun to dramatically cut the cost of its systems. It integrates a CPU, FPU, MMU, 6K of cache, a DRAM controller, and an SBus interface onto a single chip. With roughly the same performance as a 486DX2-50, microSPARC targets the low end of the workstation market.

The chip gets its award for coming in at 225 mm^2,

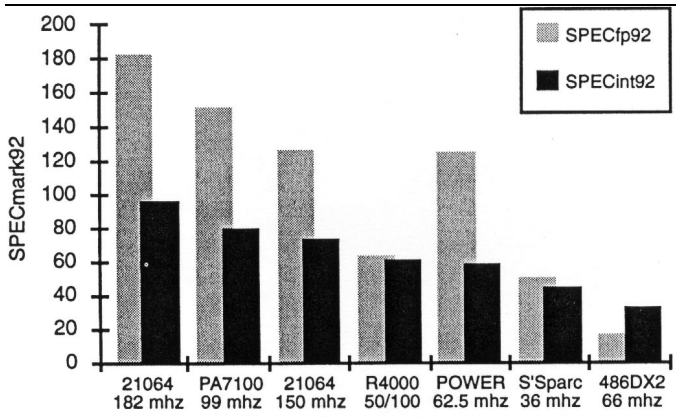

Figure 1. SPECmark92 results sorted by integer performance.

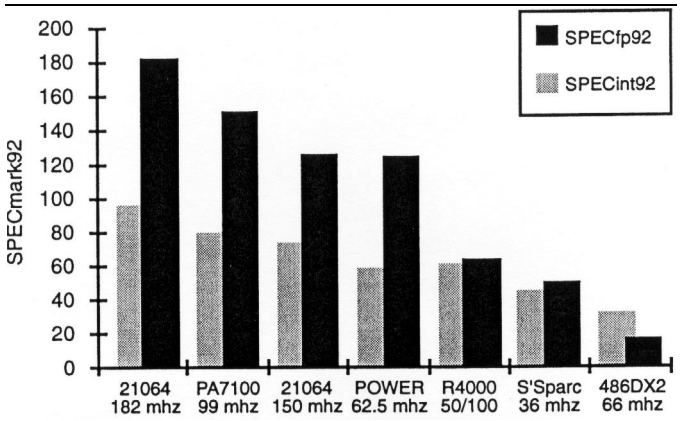

Figure 2. SPECmark92 results sorted by floating-point.

Processor	DECchip 21064	HP PA7100	IBM Power 6264	MIPS R4000SC	TI SuperSPARC	TI microSPARC	Intel 486DX2
Pipeline Frequency (max)	200 MHz	100 MHz	62.5 MHz	100 MHz	40 MHz	50 MHz	66 MHz
Number of Pipe Stages	7	5	6	8	4	5	5
Max Instructions per cycle	2	2	4	1	3	1	1
On-Chip I-Cache	8K	none	32K	8K	20K	4K	8K
On-Chip D-Cache	8K	none	none	8K	16K	2K	unified
Peak On-Chip Cache B/W	3200 MB/s	n/a	1000 MB/s	1200 MB/s	960 MB/s	400 MB/s	1067 MB/s
Off-Chip I-Cache (max)	32M	1M	none	4M	2M (5)	none	512K (5)
Off-Chip D-Cache (max)	total	2M	64K (2)	total	unified	none	unified
Peak Off-Chip Cache B/W	1067 MB/s (1)	1600 MB/s	500 MB/s	800 MB/s	320 MB/s (1)	n/a	133 MB/s (1)
Bus Frequency (max)	67 MHz	67 MHz	62.5 MHz (3)	50 MHz	40 MHz	50 MHz (3)	33 MHz
Peak Bus Bandwidth	1067 MB/s (1)	267 MB/s	1000 MB/s (3)	400 MB/s	320 MB/s (1)	400 MB/s (3)	133 MB/s (1)
Total TLB Entries	48 entries	136 entries	144 entries	48 entries	64 entries	32 entries	32 entries
Virtual Address Space	43 bits	48 bits	52 bits	42 bits	40 bits	40 bits	48 bits
IC Process Type	CMOS	CMOS	CMOS	CMOS	BiCMOS	CMOS	CMOS
Feature Size (drawn)	0.75 µm	0.75 µm	0.70 µm	0.8 µm	0.8 µm	0.80 µm	0.8 µm
Gate Length (effective)	0.50 µm	0.66 µm	0.45 µm	0.6 µm	0.6 µm	0.65 µm	0.6 µm
Transistor Count	1680K	850K	3090K (4)	1350K	3100K	800K	1185K
Die Area	234 mm2	196 mm2	367 mm2 (4)	184 mm2	256 mm2	225 mm2	81 mm2
Package	431 pin PGA	504 pin PGA	3 × 304 pin PGA	447 pin PGA	293 pin PGA	288 lead TAB	168 pin PGA
List Price (if applicable)	$1096 (6) in 1000s	not applicable	not applicable	$700 (7) in 1000s	$1899 in 1000s	$179 in 10,000s	$600 in 1000s

(1) Uses single bus for cache, memory, and I/O—the figures shown are for that single bus
(2) Requires custom IBM cache chips with built-in cache control logic
(3) Uses separate buses for memory and I/O—the figures shown are for the memory bus only
(4) Total for three chips (does not include cache control logic in custom cache chips)
(5) Requires separate cache control chip—not included in transistor count or die size
(6) 150-MHz pricing
(7) Varies among six MIPS chip vendors by about $100 plus or minus

SOURCE: Chip vendors

Table 1. Key design parameters for the top RISC processors and the 486DX2. See Table 2 for performance data.

about 2.5× the size of the aforementioned 486 (see Table 1). MicroSPARC is nearly the size of its big brother, SuperSPARC, despite using only 800,000 transistors. As described by one of the chip's designers, "there's a lot of room for improvement here."

MicroSPARC is also the first major microprocessor to use a TAB (tape automated bonding) package exclusively. TAB offers lower cost and better electrical characteristics than conventional PGA or PQFP packages, but until recently, most board manufacturers did not have the equipment to handle TAB. Sun is using the TAB package in its SPARC Classic system, and TI claims that other vendors will follow suit.

Biggest Big Microprocessor—RS/6000. IBM continues to improve the performance of its RIOS chip set, which first debuted in 1990 at 25 MHz. After two process shrinks and a quadrupling of the instruction cache size, the venerable chip set (dubbed the 6264 in this iteration) has reached 62.5 MHz. It is still essentially the same design as the original version but now offers more than three times the performance. Despite its impressive half-micron IC technology, IBM hasn't bothered to reduce the chip count, leaving the processor spread across three chips plus two to four custom SRAM chips with built-in cache control logic. The RSC (RIOS Single Chip) provides an integrated solution for low-end systems, but it may be years before IBM has a single-chip processor at the high end.

Waiting for Godot Award—88110. At the 1990 Microprocessor Forum, Motorola disclosed the first details of the 88110 and said that it would be available sometime in 1991. At the 1991 Forum, Motorola was very happy with the first chips and said they would be available soon. At the 1992 Forum, Motorola didn't have anything to say about the chip, which was still officially unannounced and not shipping in volume.

While the 88110 design is very impressive from a technical standpoint, Motorola is now downplaying the chip in favor of its new PowerPC line. Both Ford and Harris have switched product lines from the 88000 family to PowerPC. The similar bus interface of the PowerPC 601 and the 88110 may convince other customers to do the same. Despite Motorola's official statements that it will support all three of its processor families across a broad range of markets, the company appears to be quietly pushing PowerPC as the choice for general-purpose systems and the 68000 family for embedded applications. This would relegate the 88110 to a minor role.

Godot Award (honorable mention)—R4000MC. The multiprocessor version of the R4000 was originally intended to ship early this year with the rest of the family, but the MC has been plagued by bugs, despite several chip turns. Now it appears that the chip may be obsolete before it ever ships; the next-generation R4400MC should be ready next spring.

Biggest Non-Event—Pentium. Since Intel

System	DEC 7000 Model 610	DEC 3000 Model 500	HP 9000 Model 735	RS/6000 Model 980	SGI Crimson	SPARCstation 10 / Mod. 30	SPARC Classic	Compaq Deskpro/66M
Processor	DECchip 21064	DECchip 21064	HP PA7100	IBM Power 6264	MIPS R4000	TI SuperSPARC	TI microSPARC	Intel 486DX2
Clock Rate	182 MHz	150 MHz	99 MHz	62.5 MHz	50/100 MHz	36 MHz	50 MHz	66 MHz
Cache (on/off-chip)	16K/4M	16K/512K	none/512K	32K/64K	16K/1M	36K/none	6K/none	8K/256K
espresso	94.6	74.6	92.3	55.0	54.5	40.7	26.2	30.6
li	101.7	76.8	86.4	59.7	67.8	44.1	20.7	49.0
equtott	128.4	95.5	90.9	67.1	78.7	74.3	51.9	29.7
compress	62.1	49.7	66.0	51.3	69.3	26.1	18.5	20.1
sc	162.0	127.2	71.7	64.5	67.1	64.3	34.2	51.9
gcc	65.3	48.7	76.7	59.3	40.7	38.2	18.8	23.9
SPECint92	96.6	74.3	80.0	59.2	61.7	45.2	26.4	32.2
spice	87.8	60.7	91.9	73.7	44.5	32.6	17.0	19.2
doduc	125.2	102.7	142.0	88.6	51.8	39.7	17.0	15.3
mdljdp2	133.9	108.6	192.1	124.2	88.3	58.0	24.6	16.8
wave5	99.6	79.1	112.1	69.2	40.7	38.9	13.7	5.9
tomcatv	279.8	139.1	138.0	210.3	68.1	45.5	20.8	16.3
ora	152.1	125.5	276.9	103.1	73.9	105.5	31.2	22.7
alvinn	452.1	268.9	176.8	206.2	76.1	111.6	34.0	27.5
ear	551.2	447.3	258.4	174.2	89.6	66.5	28.9	28.8
mdljsp2	69.4	55.8	92.3	57.3	46.3	28.9	14.5	9.0
swm256	186.0	96.9	79.3	95.8	38.5	44.6	13.3	10.3
su2cor	264.3	141.6	177.2	208.1	75.4	45.7	25.9	19.5
hydro2d	196.5	140.7	166.1	126.7	77.5	44.9	22.3	16.3
nasa7	240.5	149.0	123.3	203.9	74.3	37.8	27.3	15.4
fpppp	176.0	141.2	237.1	172.6	77.5	49.4	16.9	18.1
SPECfp92	182.1	126.0	150.6	124.8	63.4	49.4	21.0	16.0

Table 2. SPECmark92 results for the top RISC processors shipping today and the fastest 486. (The PA7100 is currently at 96 MHz instead of 99 MHz.) All results are from vendors' official SPEC submissions.

claims that Pentium uses the same design techniques (single-cycle execution, superscalar dispatch) as its RISC competitors, it gets an honorary RISCie award. But for 1992, Pentium created much ado about very little. Major technical disclosures turned into overviews of the chip design, as Intel refused to answer most questions. The announcement itself was pushed into 1Q93, supposedly to synchronize with the system vendors' schedules. Intel continues to generate vast amounts of publicity for the unannounced chip, even issuing a press release solely to announce the Pentium name. Other vendors plan to call their compatible chips "586."

As we wait for Intel to provide more information, rumors abound that Pentium chips have poor yield at their target frequency of 66 MHz, that massive heat sinks and/or fans are required to cool them, and that the 1Q93 introduction date is in jeopardy. One thing we do know is that Pentium is monstrously large, exceeding even SuperSPARC in die size. Intel's legions of engineers continue to work on the problems, and the company assures us that everything is under control.

Most Likely to Phone Home—Hobbit. At the other end of the scale, AT&T announced a pint-sized processor that packs the power of a 486. The company hopes to create a new market for portable personal communicators that integrate computer and wireless communication functions. EO has already announced such products using Hobbit, and both NEC and Toshiba promise to follow suit. If these companies succeed in their plans, sales of these communicators could dwarf personal computer sales by the end of the decade.

Smallest Chip with a Big Design Win—ARM. At just 80 mm^2, the ARM600 CPU retains its title as the world's smallest RISC chip. More importantly, it was selected by Apple as the core of its forthcoming Newton product, a handheld personal organizer. Both ARM and Hobbit now have the opportunity to set new standards for personal computing, breaking the stranglehold that the x86 has held for the past decade.

LaserJet 4 Award—i960. In a closely fought battle, Intel's 960 edged AMD's 29000 for this coveted high-volume socket at the heart of HP's new LaserJet product line. Both of these chip families continue to do well at the high end of the embedded controller market, in products such as laser printers, X-terminals, and network routers. Opportunities have been more limited in the high volume, low cost portion of the embedded RISC market; the LaserJet 4 is the biggest win yet for RISC vendors in this area.

Most Embedded RISC Chips—IDT. Integrated Device Technology had an active year, expanding its MIPS-based 3051 family with the 3081 at the high end and the 3041 at the low end. The 3041, shipping in early 1993, will cost just $15 in volume, a price point that may pump up the volume in the embedded RISC market. IDT is also funding a chip from QED called Orion. (QED,

The Name Game

The 21064 microprocessor takes the award for the most forgettable name. DEC explained that the "21" stands for 21st-century computing, and the "64" is for the 64-bit architecture. The latest word is that the next Alpha chip will be marketed as the 21066—figure that one out!

The PA7100 gets a special award for actually having a name; HP has neglected to provide an official name for any of its previous PA-RISC implementations. By the way, an HP source explained the chip name as indicating the 7th PA-RISC processor running at 100 MHz, but HP's next chip, which runs at up to 75 MHz, will be called the 7100LC, not the 8075.

Intel has the most confusing names. It abandoned the simple numeric progression of the x86 line for "Pentium," which sounds like a chewing gum. Is "Pentium-SX" soon to follow? The random alphabetic extensions of the i960 product line have been confusing us for years.

MicroSPARC edges SuperSPARC for most annoying name; both are too long to fit neatly in charts, but microSPARC is also confusing with its capitalization, or lack thereof. Thank goodness for straightforward names like the R4000 and 88000 families!

founded by former MIPS employees, is an independent processor-design house.) Orion will be useful in high-end embedded applications as well as in Windows-NT systems, but it isn't expected to ship until early 1994.

Most Likely 1993 Casualty—i860. Actually, this award is a tie with the 88110, which was discussed earlier. The British royal family had a bad year, but the i860 has seen its last remaining system vendors either withdraw from the market (Oki), switch to another CPU (Stratus), or go into bankruptcy (Alliant). This leaves the chip in a niche market as a 3D-graphics accelerator and as the CPU in Intel's massively-parallel supercomputers. (This product has made Intel the top vendor of such systems.) Like Motorola, Intel is trying to support three different CPU architectures, and probably needs only two. The x86 is the flagship CPU, and the i960 has done well in the embedded market. Intel may have to build an x86-based supercomputer before it can terminate the i860. ♦

Major RISC Events of 1992

IDT's R3081 Adds FPU, Larger Cache to R3052 *(see **060103.PDF**)*; R3041 Lowers MIPS Embedded Entry Cost *(see **061508.PDF**)*.

DEC Enters Microprocessor Business with Alpha - *(see **060301.PDF** and **061506.PDF**)*.

MIPS and Silicon Graphics Merge *(see **060401.PDF**)*, MIPS Lays Out R4000 Roadmap *(see **060502.PDF**)*, R4400 Offers 60%–80% Performance Boost *(see **061503.PDF**)*.

HP Reveals Superscalar PA7100 Design *(see **060406.PDF**)*, Forms PA-RISC Support Organization *(see **0605MSB.PDF**)*, Takes Performance Lead with PA7100 *(see **0613MSB.PDF**)*.

Cypress/Ross Previews Pinnacle Design *(see **060405.PDF**)*, Announces "HyperSPARC" *(see **060701.PDF**)*.

SuperSPARC Premieres in SPARCstation 10 *(see **060701.PDF** and **060702.PDF**)*.

IBM Announces 100-SPECmark RS/6000 *(see **0607MSB.PDF**)*, followed by 62.5-MHz POWER *(see **0613MSB.PDF**)*.

SPARC International Announces V9 Specification - *(see **0609MSB.PDF**)*.

Windows NT Offers RISC a Chance on Desktop *(see **061001.PDF** and **061102.PDF**)*.

IBM Delivers First PowerPC Microprocessor *(see **061401.PDF**)*.

SPARC Hits Low End with TI's microSPARC *(see **061402.PDF**)*.

AT&T's Hobbit Enables Personal Communicators *(see **061403.PDF** and **061509.PDF**)*.

ARM250 Integrates RISC System on a Chip *(see **061404.PDF**)*.

Low End PA7100LC Adds Dual Integer ALUs *(see **061504.PDF**)*.

"Orion" MIPS Chip Targets Windows NT Boxes *(see **061507.PDF**)*.

