MIPS R4400 Offers 60-80% Performance Boost

Second-Generation R4000 Doubles Cache Size, Increases Clock Rate

By Michael Slater

MIPS Technologies Inc., the chip design and licensing division of Silicon Graphics, has announced the next-generation R4000, now christened the R4400. The R4400 was previously called the R4000A; it is an R4000 with twice the on-chip cache (32K total), implemented in 0.6-micron CMOS, and offered at clock rates up to 150 MHz internal (75 MHz external). Versions specified for 50/100 MHz and 67/133 MHz operation will also be offered.

Like the R4000, there are three versions of the part, differing only in their packaging and testing: the R4400PC (primary cache only, in a 179-pin PGA), R4400SC (with secondary cache interface, in a 447-pin PGA), and R4400MC (for multiprocessor systems, also in a 447-pin PGA). Each version is pin-compatible with the corresponding R4000 version, allowing existing systems to be easily upgraded.

The R4400 will be the first R4000 processor to be shipped in a fully qualified multiprocessor (MC) version. The R4000MC still has some bugs, and most (if not all) multiprocessor system vendors are expected to wait for the R4400MC for production systems. The R4400 is also the first version of the R4000 for which the master/checker mode is fully functional.

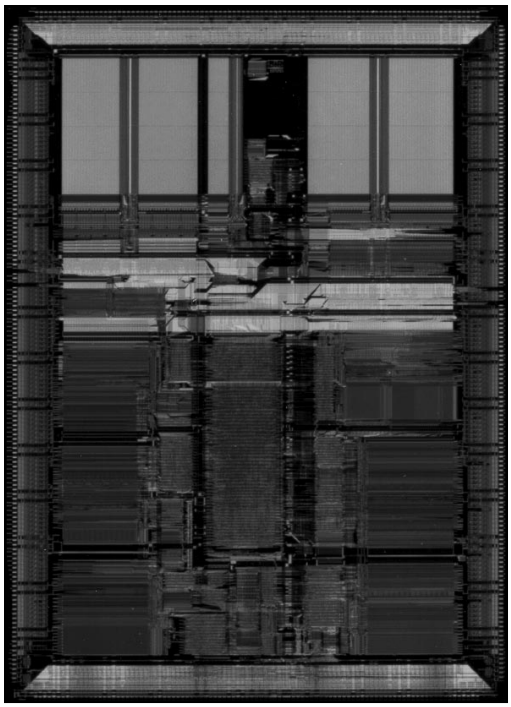

Figure 1. Die photo of the R4400, which includes 2.2 million transistors on a 15.5 × 11.9 mm (610 × 470 mil) die.

The R4400 packs 2.2 million transistors onto a 15.5 × 11.9 mm die, as shown in Figure 1. Even with the doubled cache size, the design is pad-limited in the 0.6-micron, two-level-metal technology; the core size is 15 × 10.5 mm.

Both 3.3V and 5V versions will be available. Power dissipation at 150 MHz with a 5V supply is about 20 W; the 3.3V version cuts this to about 10 W. Vendors don't expect any clock-rate compromises in the 3.3V devices. The 3.3V devices use a different process (with a thinner gate oxide) and a slightly different mask set (with smaller gates) to optimize for lower-voltage operation.

The 3.3V version has 3.3V I/O, so it requires system-logic ASICs that run at that voltage. Some system makers will use the 5V version of the R4400 so they can easily retrofit existing R4000 designs; 3.3V systems will require more engineering. Typical 3.3V system designs will translate signals to 5V levels in the system-logic ASICs so 5V DRAMs can be used. Most troublesome for high-end 3.3V systems is the lack of suitable SRAMs for the second-level cache, which also must operate at 3.3V.

Since the R4400 is about the same die size as the R4000 (albeit in a slightly more expensive process), it may obsolete the R4000 fairly quickly. The 75/150-MHz version of the R4400 will carry a significant price premium, but some vendors expect to price the 50/100-MHz R4400 competitively with the R4000.

Table 1 shows the simulated SPEC89 ratings for the R4400, along with measured figures for the R4000. (The R4000SC ratings are for the SGI Crimson, while the R4000PC figures are for the ARCSystem 100.) The R4400SC ratings assume a 1-Mbyte secondary cache, and both R4400 ratings assume a high-performance memory system. (No measured performance figures or SPEC92 ratings for the R4400 were available as of press time.)

With a secondary cache, the 75-MHz R4400SC is about 60% faster than a 50-MHz R4000SC. The performance boost is greater than the 50% clock-rate increase because of the larger on-chip cache. Without a secondary cache, the boost is even greater; the 75-MHz R4400PC is over 80% faster than a 50-MHz R4000PC. Some of this boost may be due to different memory system and compiler assumptions, however.

Other than the larger cache, the only major new feature in the R4400 is the addition of a single-level write buffer for non-cached writes. This feature was added primarily to improve graphics performance by allowing the processor to continue operation while a frame-buffer write is pending. In the R4000, the pipeline stalls on any uncached write until the bus transaction is completed. On the R4400, the pipeline continues executing past a write, as long as the write buffer is free. Assuming a full-speed bus, sequential writes can occur without stalls if

	R4400SC	R4400PC	R4000SC	R4000PC
gccl	74.4	54.1	45.2	28.5
espresso	88.4	72.0	55.4	40.5
spice2g6	73.0	43.0	45.9	24.8
doduc	82.2	65.5	52.8	36.3
nasa7	145.0	81.6	94.2	43.4
li	105.0	83.2	67.8	45.8
eqntott	123.0	100.0	79.2	45.3
matrix300	391.0	286.0	244.6	172.1
fpppp	97.5	62.1	57.7	32.7
tomcatv	123.0	73.8	68.8	37.4
SPEC89mark	113.0	79.2	70.4	42.8
SPEC89int	95.3	75.5	60.6	39.9
SPEC89fp	126.0	81.8	77.8	44.9

Table 1. Simulated SPEC89 results for the R4400.

there are at least seven other instructions between the two writes.

Other minor changes have been made to the R4000 design. The divisor used to produce the bus clock from the internal processor clock can now be 6 or 8, in addition to the 2, 3, or 4 supported by the R4000. Minor changes have been made to certain error-handling facilities and status outputs.

Announced just over one year after the R4000, the R4400 demonstrates that the rapid scaling of cache size and clock rate that MIPS has promised will indeed occur. Since the logic changes to the R4000 design are minor, the risk of bugs is small. The next step, planned for the second half of next year, is the R5000, which will double the cache size again, increase the on-chip clock rate to 200 MHz, and add branch prediction. While this path might not keep up with leading-edge HP PA-RISC and Alpha implementations, especially on floating-point applications, it should keep the MIPS architecture well ahead of the x86 line and probably ahead of SPARC as well. ♦

Price & Availability

Each of the MIPS semiconductor partners has a slightly different schedule for introduction of the R4400. Toshiba is the most aggressive, promising samples by the end of this year and production ramping up in 1Q93. Most other vendors are planning to ship samples in 1Q93 with production in the second quarter. Most vendors are planning to provide both 3.3V and 5V versions, but Toshiba said that it is focusing primarily on the 3.3V model. IDT plans to focus first on the 5V version with the 3.3V model to follow in mid-93.

In quantities of 10,000, NEC quotes $1250 for the R4400PC, $1450 for the SC, and $1750 for the MC. Toshiba quoted prices in quantities of 5,000 at $1330, $1610, and $1860, respectively. These prices are more than twice those for the R4000; for comparison, Toshiba quoted (also in quantities of 5,000) $540 for the R4000PC and $640 for the R4000SC. IDT is quoting more aggressive pricing for the R4400 at lower clock rates; for the R4400PC, IDT quoted (in quantities of 1000) $760 at 50 MHz, $1080 at 67 MHz, and $1300 at 75 MHz; for the SC models, IDT's prices are $950, $1350, and $1620.

IDT, 408/727-6116; fax 408/492-8674.

LSI Logic, 800/451-2752 or 408/433-4288; fax 408/433-7447.

NEC, 415/965-6045; fax 415/965-6130.

Performance Semiconductor, 408/734-8200; fax 408/734-0258.

Siemens, 408/980-4500; fax 408/980-4599.

Toshiba, 714/455-2000; fax 714/859-3963.

MIPS Technologies, Inc., 415/960-1980.

