PIC Family Upgraded

Microchip's 8-bit µC Offers 250 ns Instruction Cycle

By Mark Thorson

Microchip's latest family of 8-bit microcontrollers, the 17Cxx series, is the most recent derivative of the old PIC family originally introduced by General Instruments. Microchip spun off from GI when a group of investors took the chip-making operation private in June, 1989. Today, Microchip offers the 16Cxx and 17Cxx microcontroller families, serial and parallel EEPROMs, OTP ROMs, and display drivers.

The 17Cxx family, like the 16Cxx family before it (see µPR 12/89, p. 20), is touted as a RISC processor. However, the processor has none of the distinguishing features found in traditional RISCs, such as a load/store architecture, pipelined execution, or three-operand instructions. Microchip claims single-cycle instruction execution, but this is only true when a cycle is defined as four ticks of the oscillator clock. If RISC is taken to mean "modern architecture," which is perhaps its most consistent use, the 17Cxx is definitely *not* a RISC.

Putting the bogus RISC claim aside, the 17Cxx series does offer a fast instruction cycle time (250 ns at 16 MHz), with 20, 25, and 32 MHz versions under development. This compares well against the fastest 8-bit processors, such as NEC's K2-series and Hitachi's H8, which have minimum instruction times of 333 ns at 12 MHz and 200 ns at 10 MHz, respectively. This comparison slights the 17Cxx family, however, because virtually all of its instructions operate at this speed, even while accessing operands in the on-chip RAM..

CPU and Instruction Set

Figure 1 shows the block diagram of the 17C42. The 8-bit CPU reads its instruction stream from an on-chip, 16-bit-wide instruction memory. With overlapped in-

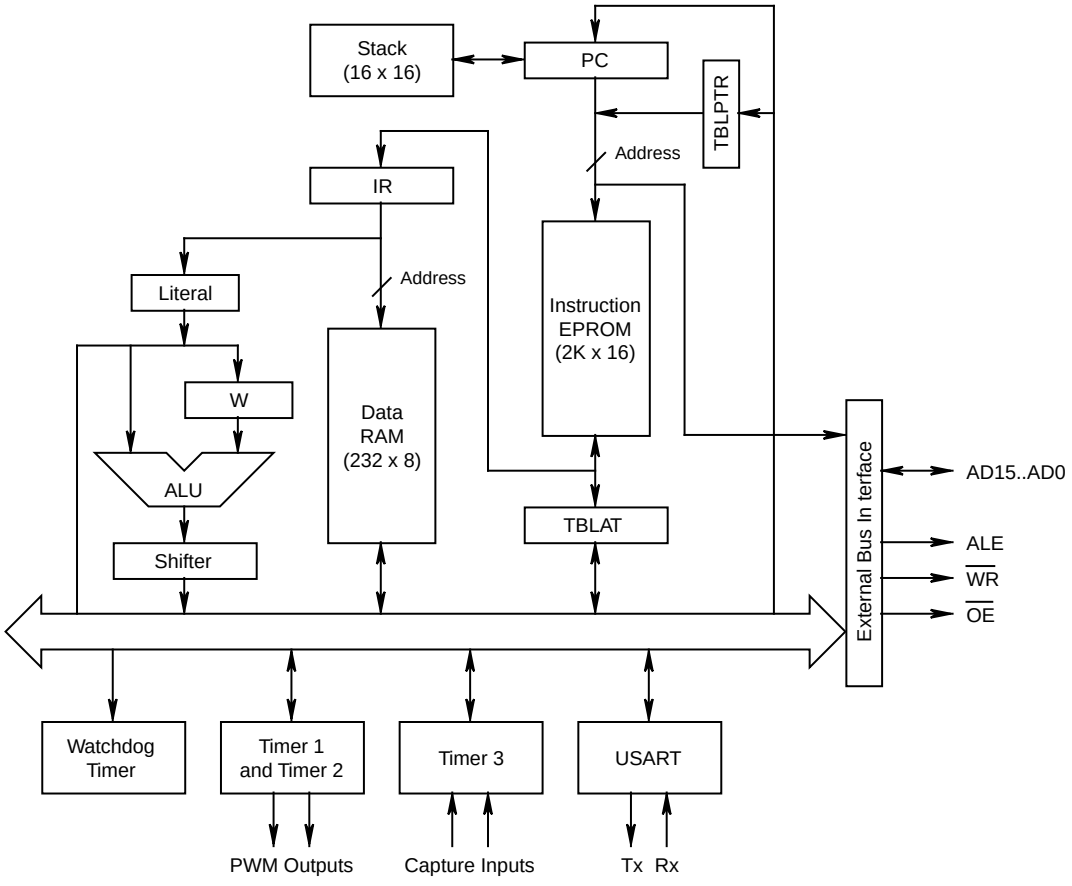

Figure 1. Block diagram of Microchip's PIC 17C42.

Price & Availability

The 17C42 is priced at $6.25 in 10K-unit volume in plastic 40-pin DIP and 44-pin PLCC and PQFP packages. Windowed packages are $19.50 in single-unit quantity. Samples are available now, with volume production planned for February, 1992.

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struction fetch and execution, the CPU can perform almost any of its instructions in four ticks of the oscillator clock.

The instruction set is accumulator oriented, with the W register required to be either the source or destination in two-operand instructions. A typical mix of arithmetic and logical operations is provided, but there is no multiply or divide. A basic set of bit set, clear, and toggle instructions is provided, as well as bit-conditional skip instructions.

All instructions are encoded in a single 16-bit opcode word, with all of the arithmetic and logical instructions having an 8-bit field that can be either an immediate-mode constant or an address in the 256-byte data space. (The PIC 16Cxx family uses 12-bit instructions, and the original PIC devices used 10-bit instructions.) The first 17Cxx part, the 17C42, has 2K words of EPROM instruction memory. Up to 64K words of external instruction memory can be added; in this mode, 19 I/O lines are used for a 16-bit multiplexed bus and its control signals. Both internal and external EPROM can be programmed under software control when an external 13-V power supply is provided.

The data space is divided between 232 byte-wide, general-purpose registers, and 48 dedicated registers. To pack an extra 24 peripheral registers into the 256-byte address space, a bank-switching scheme is used. No external data space can be added, but there are instructions that transfer data between the program space and an 8-byte area in the data space. The program space is addressed by the 16-bit TBLPTR register, using the TBLAT register as a buffer.

There is an on-chip, 16-level stack space that is accessed only by call and return instructions. A status bit warns when the stack is full, but otherwise software has no visibility into the stack.

Interrupt call and return is fast, with worst-case interrupt latency being equal to three instruction cycles (750 ns at 16 MHz). A low-power mode is provided, in which typical active power drops from 30 mA (at 16 MHz) to 30 μA. Low-power mode is entered by executing a SLEEP instruction, and it is exited by an interrupt or reset.

Peripherals

The 17C42 has a fast USART (up to 4 Mbaud synchronous and 250 Kbaud asynchronous), watchdog timer (8-bit timer with programmable 8-bit prescaler), and three general-purpose timers. Timer 1 and Timer 2 can act as two 8-bit timers, or a single 16-bit timer. Each is equipped with compare registers, and they can be enabled to drive two PWM outputs. Timer 3 has two capture registers, which are typically used for tracking shaft rotation.

There are 33 parallel I/O lines with bit-level control over data direction. When an alternate function, such as the external bus, is enabled, the data direction bits are "don't-cares." Although the 17C42 is offered in 40-pin DIP and 44-pin PLCC and PQFP packages with functions similar to the popular 8048 and 8051 microcontrollers, there is no pinout compatibility with either device.

Development Tools

The PIC17Cxx series is supported by the PICMASTER-17 development system. This includes the PC-based PICMASTER in-circuit emulation unit with a 17Cxx personality pod (a 16Cxx pod is also available), the PROMASTER device programmer, and a Windows-based macro assembler software development environment. The PICMASTER-17 kit costs $2,995 and is planned for availability this month.

Conclusion

Although the speed is in the ballpark with high-end 8-bit microcontrollers such as NEC's K-series and Hitachi's H8, the CPU and peripheral architecture is more like low-end chips such as Intel's 8048 or TI's TMS7000. Only 232 bytes of the on-chip RAM are usable as data memory, and no external data memory may be added. Up to 64K words of external instruction memory may be added, but exchange of data between instruction and data memory is very awkward. The stack is fixed at 16 levels. The peripheral architecture lacks an A/D converter and the on-chip ROM is small. The chip's key asset is its low price; the PIC family is one of the few low-end microcontrollers produced by a U.S. supplier.

Microchip sees their part as being competitive in computation-intensive applications, such as digital servo loop control, high-speed peripheral controllers, and communication interfaces. ♦