

AT A GLANCE

**Klamath Extends P6 Family** . . . . . 1  
 Intel has unveiled details of its forthcoming Klamath processor, which includes 16K caches twice the size of Pentium Pro's, a half-speed external cache, enhancements for 16-bit code, and MMX capabilities similar to P55C's. At clock speeds of up to 266 MHz, the chip should outperform Pentium Pro as well as competitors such as K6 and M2. The reduced cost of the new part, due in 2Q97, will allow Intel to bring the P6 into mainstream PCs, but probably not until 1998.

**Editorial: Is It Soup Yet?** . . . . . 3  
 Sometimes it's hard to tell when a microprocessor has achieved volume production. The R10000 and particularly UltraSparc-2 have followed a rocky road before reaching this milestone.

**Most Significant Bits** . . . . . 4  
 MoSys and Rambus bury hatchet; Samsung proposes next-generation SDRAM; Intel 430TX spans notebook, desktop; Intel's i960RD hits 66 MHz; Silicon Magic merges DRAM and 2D graphics; RISC growth slowed in 1996.

**Intel Puts P55C on Mobile Module** . . . . . 9  
 Intel's Mobile Modules simplify notebook design by putting all processor-specific components onto a small daughtercard. The first modules feature the P55C, but future compatible cards will allow designers to move quickly into the P6 generation.

**Arthur Revitalizes PowerPC Line** . . . . . 10  
 The latest design from the PowerPC partners, code-named Arthur, combines features from the 603, 604, and 620. The result is a chip that outperforms the 604e on most applications, particularly under Mac OS, but has the low cost and low power of the 603e. Arthur, due around mid-1997, is likely to displace the 604e from Apple's line and will offer performance upgrades to current 603e-based systems.

**TI's New 'C6x DSP Screams at 1,600 MIPS** . . . . . 14  
 Texas Instruments has developed a radical DSP built around an eight-way VLIW core capable of sustaining 5 to 10 times the performance of today's leading DSPs. The TMS320C6201 aims to reach speeds of 200 MHz when it first appears in 3Q97.

**DanSoft Develops VLIW Design** . . . . . 18  
 A startup in Slovakia has revealed a four-way VLIW instruction set designed for general-purpose and embedded CPUs. The architecture reveals some interesting techniques likely to be used in future VLIW processors such as Intel's Merced. DanSoft is seeking a fab partner for its innovative design.

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