

At A Glance

Sun, Xerox to License XDBus Technology	1
Sun and Xerox have developed a very competitive high-end bus for systems with multiple processors. XDBus uses GTL transceivers and packet-switching technology to achieve high performance. The first system to use this bus is Sun's SPARCcenter 2000. The two companies are looking for licensees for the new technology.	
Editorial: Speed Kills? Not for RISC Processors	3
Recent designs, such as SuperSPARC and the 88110, indicate that complex superscalar designs have lower overall performance than simpler designs such as Alpha and the PA7100.	
Most Significant Bits	4
NEC introduces VR3800 for embedded control; Thomson announces first PowerPC product; Carrera ships R4000 board for Windows NT; MIPS opens design center for NT systems; MIPS ABI reaches fruition; SI launches SPARCware ABI; LSI announces faster SBus controller.	
Comparing the New 64-Bit RISCs	11
The MIPS, Alpha, PowerPC, and SPARC architectures have all recently developed specifications for 64-bit addressing. In making this transition, several vendors added new performance enhancements as well. Although the new extensions all provide adequate 64-bit support, each of these architectures is slightly different.	
General Magic Outlines Alliances, Product Plans	17
General Magic's "Magic Cap" software will run on personal communicators using a Motorola 68300-family processor, giving Motorola CPUs an entry into the PDA market.	
DRAMs for New Memory Systems (Part 2)	18
Rambus and RamLink use revolutionary DRAM interfaces that will force a total rethinking of memory system design, but these new parts offer much higher bandwidth than current DRAMs.	
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MicroDesign Resources
874 Gravenstein Hwy. So., Suite 14
Sebastopol, California 95472
707/823-4004 • Fax 707/823-0504

Customer service e-mail: cs@mdr.ziff.com
MCI mail: 346-0177

Publisher and Editor-in-Chief

Michael Slater
e-mail: mslater@mdr.ziff.com

Senior Editor

Linley Gwennap
408/720-8840 • Fax 408/720-9465
e-mail: linley@mdr.ziff.com

Associate Editors

Brian Case
Mark Thorson

Customer Service: Colleen McMillen

Office Manager: Lynn Rodriguez

Production Manager: Ron Liskey

Production Artist: Rachel Dufour

Contributing Editors

Dennis Allison	Rich Belgard
Mike Feibus	Bruce Koball
George Morrow	Bernard L. Peuto
John Snell	Nick Tredennick
John F. Wakerly	John H. Wharton

European Operations

Phil Sutcliffe, Parkway Gordon
Phone 44 (0)491 875386
Fax 44 (0)491 875524

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