

### ■ IC, You See, We All See ISSCC

New advances in microprocessor design, among other areas, will be in evidence at the **International Solid-State Circuits Conference (ISSCC)** to be held next February 6–10 in San Francisco. The main conference, Monday through Wednesday, features sessions on comm chips, image sensors, memory chips, signal processing, clock distribution, and, of course, microprocessors. There will also be several 90-minute tutorials on Sunday and a short course on wireless networking circuits on Thursday.

The Monday afternoon session features a 1-GHz 21264, a 780-MHz PowerPC G4, a 600-MHz PA-8600, a 1-GHz Series/390 mainframe processor (G6), and a 1-GHz Pentium III. (Note that ISSCC clock speeds are often higher than actual product clock speeds.)

On Wednesday afternoon, the session includes papers on a 600-MHz UltraSparc-3 (more than two years after it was disclosed at Microprocessor Forum), the 200-MHz C-Port network processor, a four-processor chip from NEC, and, last but not least, Merced, aka Itanium. The abstract notes that Merced includes 25.4 million transistors and uses a 1,012-pad OLGA package, but it does not offer a target clock speed or die size.

The early (before 12/27) registration fee is \$415 for the two-day conference, \$75 for tutorials, and \$300 for the short course, with discounts for students and IEEE members. For more information or to register, access the Web at [www.sscs.org/isscc](http://www.sscs.org/isscc).

### ■ Parlez Vous Performants?

On January 10–12, the IEEE will sponsor an international symposium on high-performance computer architecture, **HPCA6**. The conference, held in Toulouse, France, features papers on CPU, cache, memory, and parallel-computer architectures. It also covers topics such as power efficiency, high availability, high-speed I/O, and real-time performance. On January 8–9, two days of workshops and tutorials will precede the symposium.

The registration fee is \$608 (FFr 3650) for the symposium and \$115 (FFr 690) for each workshop or tutorial day, with discounts for students and IEEE members. For more information, browse [www.irit.fr/ACTIVITES/EQ\\_APARA/HPCA6](http://www.irit.fr/ACTIVITES/EQ_APARA/HPCA6).

### ■ SOC It to Me

By 2004, 70% of all ASICs will be a system on a chip (SOC), and 85% of all ASICs will contain some form of licensed intellectual property (IP). So says Integrated Circuit Engineering (ICE) in its new report, evocatively titled **ASIC—System on a Chip**. The report defines SOC and its implications for the traditional ASIC model; describes its use in specific markets, products, and applications; discusses technologies and core components; and explains the enablers of the SOC business model.

The report is available in hardcopy or on CD-ROM for \$1,295. Additional copies are \$775. For more information, contact ICE (Scottsdale, Ariz.) at 480.515.9780 or [www.ice-corp.com](http://www.ice-corp.com).