Integration, Diversification Key in 1998

Embedded Processors Are Proliferating, Even As They Become More Diverse

by Jim Turley

Integration and variation were the themes in 1998. Embedded-chip makers integrated more peripheral logic onto their microprocessors, and microprocessor architectures became even more varied as signal-processing, media-processing, and code-compression extensions were added.

Some of the year's developments were as predictable as a Boris Yeltsin cardiogram. Motorola's 68K dominated 32-bit sales; RISC gained ground on the older families; growth rates slowed in a turbulent economy; and vendors scrambled to tie their products to the Internet, Java, or both.

Worldwide volume of 32-bit embedded CPUs grew a respectable 25%, to more than 236 million units. ARM was the big winner, more than quadrupling its volume and overtaking SuperH to run neck and neck with MIPS.

The top clock speed for embedded chips edged up only 29%, from 233 MHz (StrongARM-110) at the end of 1997 to 300 MHz (the RM7000 and EC603e) at the close of 1998. This past year also saw a handful of 0.25-micron parts (the VR5464, K6E, and Pentium/MMX) debut in the embedded market, scant months after the technology appeared in mainstream desktop processors. The process gap between desktop and embedded processors continues to close.

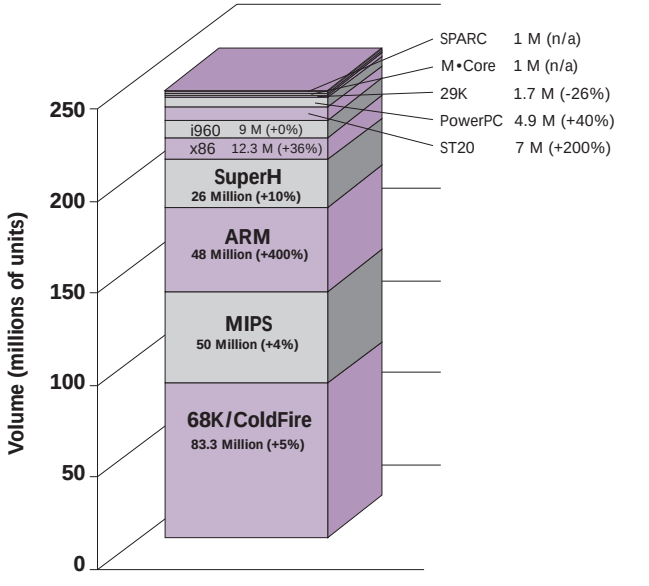

Figure 1. Total volume of 32-bit embedded microprocessors grew to 236 million units in 1998, an increase of 25% over 1997. ARM and SuperH swapped positions, while Motorola's 68K retained its traditional lead. (Source: vendors, MicroDesign Resources)

Motorola Divides and Conquers

The deathless 68K retained its embedded volume crown, with 83 million 680x0, 683xx, and ColdFire chips in 1998, up just 5% from the previous year. Once again, Motorola traded mightily on the near-eternal life spans of so many embedded systems and the docile fealty of thousands of embedded designers.

The ColdFire subspecies evolved steadily in 1998, with new chips shipping and the v4 microarchitectural changes announced, including branch prediction and fixed-point fractional-numeric support. This is probably as close as ColdFire will come to a true floating-point unit for some years, to prevent cannibalization of 68040 and '060 sales.

For integer work, the whole ColdFire family is a bargain, with a measure of 68K compatibility thrown in for good measure. (Motorola finally granted ColdFire the binary compatibility many potential users assumed it already had, through a 68K emulation library.) The 5307, in particular, offers a core set of peripherals and a sizable cache, coupled with the fastest ColdFire CPU to date, all for about $15. This valuable combination earns Motorola's ColdFire 5307 the Editor's Choice award for best integrated processor.

Pacing ColdFire progress is Motorola's "other other 32-bit processor" franchise, M•Core. With Mighty Mouse leading the way, M•Core can save the day for Motorola's wireless and automotive products. Applications too power-sensitive for ColdFire or too demanding for 16-bit chips can turn to M•Core, a family designed to compete head-on with ARM. Unlike ColdFire, M•Core will soon get true FP support.

Motorola now faces a dilemma positioning its own product lines. ColdFire and M•Core are not vastly different, at least not in any obvious way. With M•Core endowed with FP, and with other extensions on the way, it looks more and more like a competitor for ColdFire. Unfettered by any need for backward compatibility, M•Core should achieve any performance level ColdFire can reach, if not higher. Although it's a bit younger and has yet to prove its worth, M•Core is beginning to turn heads as an alternative for developers.

PowerPC Splits, Grows, Splits Again

The PowerPC partners had a relatively restrained year of growth. A far cry from the 3× to 5× growth rates of previous years, total PowerPC volume increased by a more modest 40% in 1998, to about 4.9 million embedded chips. IBM pulled ahead of Motorola, accounting for 2.8 million of that total. IBM's less-expensive processors helped its volume, while Motorola's more-expensive MPC860 communications controllers aided its revenue.

The midpoint of the year betokened bad news for the PowerPC faithful as the egalitarian concordant that was Somerset faded once again into legend. That organization now belongs to Motorola, designing new embedded chips. The AltiVec media extensions, which were initially designed for Apple but belong to Motorola, will outfit future PowerPC processors for network management or media processing. None were forthcoming in 1998, but Motorola's G4, the first chip with AltiVec, should be shipping into embedded applications by mid-1999.

PowerPC got small with the introduction of CodePack, IBM's sorely needed (and typically overengineered) code-compression system. Originally developed for disk drives (where IBM is a major supplier), CodePack will likely see use in new ASICs from that company's Vermont foundry. With CodePack, PowerPC now offers an alternative to the traditionally bulky code of a 32-bit RISC. MIPS introduced MIPS-16 two years ago, and ARM has had its Thumb in place since 1996, so PowerPC has a few years of momentum to overcome.

Of the major RISC architectures, only SPARC and the i960 remain without a compression scheme, a situation that is likely to persist *ad infinitum*. CISC architectures, such as the 68K and x86, have naturally dense code and thus no need for such technological trickery.

A record of sorts was set in 1998. The largest PowerPC chip ever, and the biggest chip in Motorola corporate history, shipped in July: the MPC555. This lowly engine controller owes its majestic size (150 mm^2) to nearly half a megabyte of on-chip memory (flash and SRAM). Hitachi, however, took the prize for most on-chip flash memory with its SH7055, which boasts 512K of flash and 32K of SRAM, with a small SH-2E processor squeezed into the spare silicon.

Motorola cemented its position as the preeminent supplier of intelligent communications controllers, adding the MPC8260 and several more MPC850 derivatives to its already intimidating arsenal. Now, with more than two dozen network- and telecommunications-related processors, Motorola has built a nearly insurmountable wall around this small but high-margin market territory.

This doesn't keep other competitors from trying, of course. AMD launched two 186-based communications controllers, the first modest barrage in what may become a protracted battle. The new chips are a reasonable brand extension for AMD, which already ships lots of Ethernet and line-card silicon. Still, without any corollary to Motorola's communications-processor module (CPM) to manage network traffic, AMD's single-threaded controllers are doomed to remain at the low-performance—and low-margin—end of the communications spectrum.

Intel Feigns Death With i960, StrongArm

This past year marked the official absorption of Digital Semiconductor by Intel. After some apparent uncertainty, Intel adopted StrongArm as one of its own. Customers—and competitors—concerned about Intel's effect on the product

Motorola Courting Foundries

As part of its most recent reorganization, Motorola's Semiconductor Products Sector (SPS) has collapsed its product organization and profoundly altered its chip-making plans. Semiconductor operations deflated from 23 product groups into just four. Some were reorganized, some were sold, some were eliminated. Among the fallen were optoelectronics, DRAMs, chemical sensors, gate arrays, FPGAs, and power electronics.

The four surviving groups are now organized around transportation, wireless, networking, and imaging/entertainment. (Discrete components are handled through a fifth independent group.) The transportation group oversees M•Core; StarCore DSPs are part of the wireless group; imaging owns 68K/ColdFire; and PowerPC is the responsibility of the networking group.

Under the new plan, called Standardize & Simplify, Motorola will consolidate its fabrication processes and rationalize its design rules. It will sell off, rather than refit, older fabs that do not match its current 8-inch production processes. Motorola has already closed plants in California, Texas, Arizona, North Carolina, the Philippines, and elsewhere. The plan parallels Intel's famous Copy Exact policy, where semiconductor plants are interchangeable.

Standardize & Simplify extends beyond Motorola's own fab equipment. By next year, 30% of production is slated to go to external foundries. Over the next three years, Motorola will shift half of its production to foundries. This is a huge strategic redirection for a company that currently farms out only 6% of its production.

Regarding the much-ballyhooed copper process, Motorola vowed to ship more chips using copper interconnect in 1999 than any other vendor, including IBM.

Motorola will not build any new fabs "for some time," according to company executives, and the next one it does build will run huge 300-mm wafers. It's likely such a plant will be a joint venture with AMD or Siemens (both of which have process-level agreements with Motorola), possibly located in Dresden, Germany.

To reconcile the seemingly conflicting goals of standardizing its semiconductor process and pushing work out to foundries, Motorola will "engage in partnerships" with foundries around the world, outfitting them for Motorola-compatible processes. Such Motorola-assisted foundries are hoped to be interchangeable with Motorola's own plants. Chips made at one location will be manufacturable at any other.

This scheme represents a Faustian bargain for the foundries. They must accept and adapt to Motorola's processes. On the other hand, they will (collectively, at least) take 50% of Motorola's mammoth production.

Embedded Events of 1998

Motorola networked with the MPC8260 (9/14/98, p. 12) and the MPC850 chips (3/30/98, p. 12). The MPC8240 got PCI (11/16/98, p. 10). ColdFire v4 (10/26/98, p. 30) and 5307 were announced (2/16/98, p. 11).

The first (MMC2001) and the second (MMC2080) M•Core chips were announced (3/30/98, p. 13) (9/14/98, p. 14), while the M300 architecture was revealed (12/7/98, p. 16).

The AltiVec PowerPC instruction-set extensions were shown (5/11/98, p. 1) as the embedded PowerPC EC603e hit 300 MHz (6/22/98, p. 11).

Motorola announced (2/16/98, p. 10), then canned, the Core+ FPGA line (7/13/98, p. 14) and swapped technology with AMD (8/3/98, p. 10). The StarCore DSP work with Lucent was announced (10/26/98, p. 22).

Intel stood behind StrongArm (3/9/98, p. 5) and revealed plans for SA-2 (8/3/98, p. 11). The SA-1100 companion chip entered production (10/26/98, p. 20).

The i960 RM, 'RN debuted (9/14/98, p. 11) as the i960JT reached 100 MHz (3/30/98, p. 8).

AMD competed for communications design wins with the 186CC (6/1/98, p. 14) and 'CH (10/26/98, p. 21).

MIPS went public (4/20/98, p. 1) amid revelations of reliance on Nintendo (6/1/98, p. 10).

Lexra announced the LX4080 core (2/16/98, p. 13), got sued (4/20/98, p. 8), and settled (10/26/98, p. 21).

NEC lowered the cost of the VR4305 (1/26/98, p. 13) and rolled out its MDMX-like VR5464 (3/9/98, p. 1).

IDT rolled out the 32364 (6/1/98, p. 12) and 64474, '475 chips (10/5/98, p. 10).

QED shipped the RM52x1 (8/3/98, p. 11), RM7000 (8/3/98, p. 12), and disclosed Alpine (12/28/98, p. 13).

SandCraft announced the SR1 (12/7/98, p. 10).

Toshiba produced an FPU-less R4300 (10/5/98, p. 5).

IBM copied TI's 'C54x DSP core (7/13/98, p. 13) and announced CodePack for PowerPC (10/26/98, p. 26).

STM and IBM swapped x86 designs (8/3/98, p. 10).

National halted in-house x86 work (2/16/98, p. 10).

Hitachi licensed SuperH to VLSI, Sony, Seiko, and NTT (4/20/98, p. 9); SH3-DSP debuted at the Forum (12/7/98, p. 10).

ARM showed cached ARM7 and ARM9 cores (4/20/98, p. 10), announced ARM10 (11/16/98, p. 14), and began work on ISA extensions (7/13/98, p. 15).

Symbian got its start (7/13/98, p. 15).

Apple killed the Newton MessagePad (3/9/98, p. 5).

EEMBC consortium was founded (4/20/98, p. 13).

Mitsubishi improved the M32R/D (8/24/98, p. 5).

Matsushita developed its MN10300 (10/5/98, p. 12).

Triscend debuted configurable E5 (11/16/98, p. 12).

Sun got its first MicroJava silicon (10/26/98, p. 20).

line needn't have worried. StrongArm remains utterly untouched by the events of 1998. In fact, the SA-110 hasn't changed since its debut in 1996. The only sign of life was the announcement of the SA-1101, a core-logic support chip developed on Digital's watch. The oft-delayed SA-1500, a complex media-processing chip, lies still on its slab, awaiting either the breath of life or the kiss of death.

Intel's "other other 32-bit processor" family, after x86 and StrongArm, soldiered bravely on. Sales of i960 chips flatlined, hovering at nine million units, unchanged from 1997. The 'RN and related I_2O processors administered first aid to the i960 line but couldn't revive flagging sales of the older members ('KB, 'CA, etc.).

Intel pitches the newer i960 chips for I_2O applications, a niche other vendors seem willing to cede to Intel. The new 'RM and 'RN supplement the original 'RP and 'RD, adding speed and tracking the inevitable changes in the PCI and I_2O specifications. Through force of will (and a 0.35-micron process change), Intel pushed the i960JT to 100 MHz, marking the first time these descendants of BiiN reached triple digits.

The coming year will show how Intel intends to position StrongArm against i960, an irksome dilemma. By any objective measure, StrongArm is superior to the medieval i960. To prevent direct comparisons, Intel will likely keep StrongArm cores away from I_2O peripherals and dual PCI buses. Future SA chips—including the SA-2 generation under development in Arizona—may instead acquire graphics, network, or core-logic features that highlight their value in portable systems, digital cameras, and set-top boxes.

AMD, Intel, STM, National Tinker With x86 Lines

The past year saw little change or news in the x86 world. AMD and Intel both gave up their previous generation of processors for adoption, moving them into their embedded families. AMD's rechristened K6E is unchanged from the original K6; Pentium/MMX (with or without an attached module) is similarly unaltered by the transition.

National Semiconductor whacked its in-house design team in favor of x86 cores from subsidiary Cyrix, and a year's worth of planned embedded chips went in the dumpster. ST (formerly SGS-Thomson) expanded its line of integrated chips to three, with the STPC Consumer, Industrial, and Client differing in quantity and mix of peripherals. Unlike National, ST is moving away from Cyrix-designed cores. Like National, it will shift to x86 designs from its newly acquired subsidiary, in this case, Metaflow.

The volume of embedded x86 chips was up 36% from the prior year, reaching over 12 million units. Intel and AMD split sales about 66/33, with STM and National getting the fractions.

SuperH Growth Slows, DSP Emphasis Increases

SuperH sales grew to 26 million units in 1998, a little over 10% growth. This is well off the previous year's 28% growth, or the *annus enormis* of 1996, when Hitachi abandoned its stealth

marketing campaign and SuperH first revealed itself in full poignant bloom. (These quantities include SH-1 chips, which some others classify as 16-bit processors.)

Hitachi continues to press its advantage in two areas, video games and handheld computers, while enthusiastically branching out into digital cameras, automotive electronics, and telecommunications. The DSP ability embodied in chips like the SH7729 has also won Hitachi friends among networking and telecommunications vendors. Cisco, for one, has demonstrated the SH7729 in a voice-over-IP cable-modem design.

Part of Hitachi's relatively slow growth can be laid at the feet of Sega, which badly bungled its marketing of the Saturn game console in North America, finally pulling the unit (which uses three SuperH processors) from U.S. shelves in March. With fully a year between the demise of Saturn and the rise of the SH7750-based Dreamcast—not to mention the 3-to-1 difference in chip count between these two systems—SuperH sales took a big hit in 1998. In this light, Hitachi's growth in unit volume is all the more admirable.

Looking ahead, Hitachi hopes to oust StrongArm from the MIPS/watt roost with a modified SH-4 core and to add PCI to some of its products. The SH-5 is still due in 2000.

MIPS Vendors Dial In Price/Performance Ratios

In the past year, MIPS chips almost universally held the performance lead, month by month. With half a dozen eager licensees actively developing newer, faster processors, the performance and price/performance leads generally went from one MIPS vendor to another as the year wore on.

Among the fastest chips of the year was NEC's VR5464 (developed with SandCraft), a 250-MHz beast that implements the nearest thing to MDMX. The MIPS partners have been surprisingly slow to deploy MDMX, given how closely their fortunes are intertwined with media processing, graphics, and consumer electronics. We expect 1999 will see the debut of the first real MDMX implementation, although no such plans have been announced.

Among the more active MIPS units was IDT, which started rolling out its "5-digit" in-house designs, the 64474 and '475 at the high end and the 32364 for the midrange. All three have excellent price/performance and are a credit to IDT's heretofore underutilized design team. Because of its efficient design, top-notch integer performance, and aggressive take-notice pricing, IDT's RC32364 earns the coveted Editor's Choice award for best price/performance.

IDT's new chips lay the groundwork for a presumed range of integrated processors. Given IDT's background, these will likely be aimed at telecom and networking applications. All in all, this is a big strategic shift for a company whose CEO graded new processors by asking, "How much RAM is on it?"

The practiced hands at QED were no less active in 1998, crafting the awesome RM7000 and the economical RM52x1 triplets. The RM5231, in particular, gives IDT's '474 more than enough competition with a combination of high speed, big cache, bargain price, and full-figured floating-point unit.

Philips has decided to exit the PDA-processor business by midyear, stranding its PR31700 chip used in the Velo and Nino. The company still plans to create new MIPS-based devices for other applications, just not for handheld systems.

ARM Lays Groundwork for Extensions

Perhaps exhausted from its peripatetic hunt for licensees, ARM remained comparatively calm through 1998, announcing one major architectural upgrade—the inspiringly named ARM10—which is due to sample in the second half of 1999.

ARM's massed hordes shipped an estimated 48 million units in 1998, a whopping 5× increase and far more growth than any competitor could show. After years of cultivating licensees, ARM seems finally to be reaping what it has sown.

New cached versions of ARM's core macros are a bow to the increasing demands of bandwidth when CPU speeds creep above 66 MHz or so. The CPU-plus-cache designs were a no-brainer from an engineering point of view, but they allow the company to sell a different (and larger) macro to its customers, and make integration a bit simpler besides.

In the area of architectural extensions, ARM is developing new instructions and debug hooks. Originally intended just for disk drives, the project has grown to encompass in its scope printers, antilock brakes, DVD, and engine management, among others. Such development is entirely symptomatic of processor design direction. Base-level ISAs are a dime a dozen; few design decisions are based on how a chip handles four-function math and Boolean decisions. Specific features, whether for signal processing, video processing, code compression, pixel manipulation, geometry setup, or servo control, are the distinguishing characteristics.

As transistors become more plentiful and synthesis tools mature, narrow application-specific extensions will be the order of the day. ARC (Argonaut) has always based its business on this thesis; its processor core flaunts its configurability, and customers have responded enthusiastically. ARM, MIPS, and even IBM are moving in the same direction, though more cautiously. The coming year will undoubtedly see new companies spring up, offering configurability at different, and perhaps unexpected, levels of the architecture.

Java Still Surrounded by Thick Clouds

The industry climate did little to dissipate the clouds surrounding Java in 1998. The most notable ray of hope arrived as Sun collected its first MicroJava 701 samples. Delivered on the first day of Microprocessor Forum, the first incarnation of Sun's PicoJava-II core has begun the lengthy process of initial test and debugging. Sun's engineers are hopeful (as they must be), while the faithful wait for the white smoke to rise from Sun's chimney. General sampling of the 701 is slated for 2Q99.

Sun reversed its earlier decision to produce a series of its own Java chips, now preferring to leave the production and marketing work to its licensees. The company will instead follow the example of MIPS, ARM, and others, developing new Java cores and licensing them to the unwary.

Unit volume of Java processors was—once again—zero. It appears that either the market for such chips has failed to materialize, or the vendors have failed to meet it. Either way, the market for Java silicon remains completely theoretical.

Those responsible for the name ShBoom redeemed themselves by recasting Patriot's unusual PSC1000 processor as "the first market-ready Java chip." Optimistic perhaps, but a sign of the times. Patriot also managed an extra 70 MHz, shipping 150-MHz 0.35-micron components.

The end of the year saw Swedish newcomer Imsys showing off its GP1000, another unusual processor that has found value in billing itself as a Java chip. The chip in no way competes with the 701; it is slower, smaller, and less expensive. But, for now, the Patriot and Imsys parts are intriguing alternatives for low-end embedded systems. In the mainstream, various CPU vendors are rumored to be toying with Java accelerators or extensions of diverse description; perhaps some will be announced in 1999.

Palm PCs Popular, But Not Because of Technology

The previous year promised a shakeup of the handheld electronic-organizer (aka PDA) market, but no serious upheaval occurred. Microsoft and its minions unleashed the Gryphon (officially the PalmPC) in the spring, hoping to grab a portion of the PDA market dominated by Psion and 3Com.

The year saw 3Com continue to dominate the hearts, minds, and breast pockets of North American consumers; Psion overrun Europe once again; Apple drop from the market entirely; Windows CE vendors scramble for differentiation; and various parties change the name of their products.

Amid a flurry of trademark lawsuits, Microsoft converted "PalmPC" to "Palm-size PC" (dropping the final "d" from the modifying phrase), while 3Com, under pressure from the eponymous felt-tipped-pen company, eliminated the much-loved "Pilot" moniker from its brand.

The motive force driving Psion's unheralded success spun off into a separate venture, Symbian, jointly owned by Psion, Ericsson, Nokia, and Motorola. The collective will try to extend the reach of its operating system, EPOC (which stands for Electronic Piece Of Cheese—really). That EPOC will appear on future cellular telephones and related devices from these vendors is a given. That ARM will benefit seems also assured, as EPOC runs only on ARM chips. Motorola, shrewdly enough, rapidly announced support for, and an effort to port, EPOC onto its own M•Core processors, giving the U.S. manufacturer a somewhat less embarrassing platform on which to run its newly acquired operating system.

Customization Becoming Key for the Future

Synthetic-processor suppliers Lexra and ARC both had good years, with the former dodging a legal bullet and the latter breaking ARM's record for most new licensees during a single orbit around the sun. Nontraditional CPU suppliers such as Xilinx, Synopsys, and Cadence also made their voices heard, offering synthesizable processors with their ASIC tool chains.

Other, somewhat more mainstream, processor vendors also took synthesizability to heart. ARM now offers synthesizable cores to selected licensees. ColdFire has always been synthesized, but now PowerPC and M•Core devices will be "compiled," along with their peripherals. As one of its first official acts, newly independent MIPS Technologies began describing a series of new processor designs, all three of which will be available in both hard and soft formats.

Triscend, which held its official coming-out party at Embedded Processor Forum, takes synthesizability in a different direction: to the peripherals. Starting with the all-too-familiar 8032 CPU core, Triscend's customers can convert uncommitted logic on the chip to peripherals on demand. Scenix Semiconductor proffers a similar promise, though it uses brute force to emulate peripheral functions with its 100-MHz processor. Newcomer TeraGen (see MPR 1/25/99, p. 9), adheres to roughly the same philosophy, running very fast processors in place of very slow peripherals.

All of these companies base their product strategy on the same underlying canon: transistors are free. And in a practical sense, that assumption is essentially true. Especially for smaller, 8-bit devices (which all of these examples are), the silicon is the least expensive part of the product. As with perfume, the packaging and marketing control the cost. If increasing transistor count and die size improve time to market or flexibility, it's silicon well spent.

The Coming Standard Is Fragmentation

Embedded sales keep growing, and there's still no shakeout in sight. On the contrary, new companies are still entering the market, and the number and type of CPU architectures keep increasing. It seems clear that no PC-like consolidation is in the cards for embedded systems. In diversity is strength.

Even existing CPU families are splitting, spinning off, or fragmenting. Optional instruction-set extensions for media-, motion-, or signal-processing functions turn a single CPU family into a collection of product choices. A single unified instruction set can't serve all applications, and vendors are responding with an smorgasbord of a la carte choices.

Synthesized CPU cores and next-generation development tools will accelerate this fragmentation. Instruction sets will be something determined by the individual developer, in front of a CAD system, not by the vendor's product staff. Even though binary compatibility will go flying out the window, the freedom to customize will blow in at the same time. Processor instruction sets are just the starting point. The end point will be up to individual embedded engineers. M