by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,740,441

Bytecode program interpreter apparatus and method with pre-verification of data type restrictions and object initialization
Issued: April 14, 1998
Inventors: Frank Yellin, et al.
Assignee: Sun
Filed: December 20, 1995
Claims: 18
A program interpreter for computer programs written in a bytecode language. The interpreter, prior to executing any bytecode program, verifies the integrity of a program by identifying any instruction that would process data of the wrong type and sequences that would cause stack overflow or underflow. Thereafter, the interpreter executes the program without type checking or stack-fault checking.

5,740,413

Method and apparatus for providing address breakpoints, branch breakpoints, and single stepping
Issued: April 14, 1998
Inventors: Donald Alpert, et al.
Assignee: Intel
Filed: July 23, 1997
Claims: 17
Methods and apparatus that enable breakpoints and/or single stepping to occur in a processor. The invention allows breakpoints to occur successfully around branches, which may switch the processor to another mode of operation.

5,737,631

Reprogrammable instruction-set accelerator
Issued: April 7, 1998
Inventor: Stephen M. Trimberger
Filed: April 5, 1995
Claims: 40
A data processor that has a defined execution unit for execution of a predefined set of instructions and a programmable execution unit for execution of a reprogrammable instruction set.

5,737,624

Superscalar RISC instruction scheduling
Issued: April 7, 1998
Inventors: Sanjiv Garg, et al.
Assignee: Seiko Epson
Filed: January 31, 1996
Claims: 19
A register-renaming scheme in a microprocessor, whereby a data-dependency checker inspects multiple instructions in an instruction window. When there are data dependencies or registers, dependent source-operand register names are replaced by tags of renamed registers that will hold the data.

5,737,613

Method of operating a microcomputer to minimize power dissipation while accessing slow memory
Issued: April 7, 1998
Inventor: William D. Mensch, Jr.
Filed: March 10, 1995
Claims: 7
Methods of operating a CMOS microprocessor where the clock speed is slowed to the speed of the main memory when the microprocessor accesses main memory to conserve power, otherwise operating at a faster speed.

5,737,562

CPU pipeline having queuing stage to facilitate branch instructions
Issued: April 7, 1998
Inventor: Robert L. Caulk, Jr.
Assignee: LSI Logic
Filed: October 6, 1995
Claims: 11
A pipelined microprocessor that has a queuing stage between an instruction-fetch stage and an instruction-decode stage to facilitate branch instructions and to receive instructions from the fetch stage when the decode stage is stalled. If a branch is incorrectly predicted taken, the queuing stage contains nonbranch sequential instructions for the decode stage, while the fetch stage is restarted at the nonbranch sequential instruction stream.

OTHER ISSUED PATENTS

5,740,461 *Data processing with multiple instruction sets*
5,740,417 *Pipelined processor operating in different power mode based on branch prediction state of branch history bit*
5,740,391 *Preventing premature early exception signaling with special instruction encoding*
5,740,093 *128-bit register file and 128-bit floating-point load and store for quadruple-precision compatibility*
5,737,625 *Selectable processing registers and method*
5,737,614 *Dynamic control of power consumption in self-timed circuits*
5,737,590 *Branch-prediction system using limited branch-target-buffer updates*
5,737,586 *Data-processing system and method thereof*