Microarchitecture on the MOSFET Diet

Kerry Bernstein
Senior Technical Staff Member
IBM T. J. Watson Research Center
Yorktown Heights, NY

Abstract

Microarchitecture and technology scaling have historically shared responsibility for the microprocessor's phenomenal generation-over-generation performance improvement. The era marked by unrestrained proliferation of successively scaled, leakier devices to achieve incremental architectural transaction rate growth is coming to a close, however. Increased pipeline depth has caused non-linear latch density expansion; shorter FO4-equivalent cycles have made control logic substantially more complex. The resulting energy per operation, scaled-process-induced delay variation, logic corruption due to soft errors, and erosion in die area access latency have become real-world constraints. This talk will explore how features of past technologies have influenced high speed microarchitectures, and how the characteristics of proposed new devices and interconnects for lithographies beyond 90 nm may shape future machine design. Given our industry's power-restricted ability to continue scaling, and the approach of fundamental, quantum-mechanical precision boundaries, the role of microarchitecture in extending CMOS performance will be more important than ever.

Proceedings of the 36th International Symposium on Microarchitecture (MICRO-36 2003)
0-7695-2043-X/03 $17.00 © 2003 **IEEE**