Message from the Workshop Chair and Program Chair

We welcome you all to the 14th Reconfigurable Architectures Workshop being part of the annual symposium on international parallel & distributed processing IPDPS 2007 held in Long Beach, California, USA.
The workshop covers a range of actual and interdisciplinary topics: new reconfigurable architectures, design methods, run-time reconfiguration, algorithms and technologies. This year the special focus is coarse grain reconfigurable. Coarse Grain architectures, methods, tools and applications are presented in several special sessions.
Over more than one decade this workshop has been an unique forum promoting multidisciplinary research and new visionary research approaches in the area of reconfigurable computing.

Future design methodologies are also one of the key topics at the workshop, as well as new tools to support them. This year we are happy to count 68 high quality submissions from 22 different countries all over the world. Based on at least 3 reviews per paper a thorough selection of 33 regular papers was done with the great support of all program committee members. In addition, two attractive keynote contributions enrich the content of this workshop. This year RAW provides an innovative platform for authors from 14 countries to present their qualified work at this workshop and to discuss it with all participants.

We would like to take the opportunity to acknowledge the effort and help from the program committee members and reviewers, and thank all authors and invited speakers for their contributions to the program. Many thanks to the steering chair Viktor Prasanna (University of Southern California) as well as to the publicity chairs Ramachandran Vaidyanathan (Louisiana State University) and Reiner Hartenstein (Kaiserslautern University of Technology, Germany) for their constant input and support of RAW 2007. Moreover, we would like to stress the great job of Oliver Sander and Michael Hübner (Universität Karlsruhe) for assisting us in all organizational matters.

We wish you a very prolific workshop and hope you will find these proceedings to be a valuable information reference for your future work.

Serge Vernalde, Workshop Chair
IMEC, Leuven, Belgium

Jürgen Becker, Program Chair
Universitaet Karlsruhe(TH), Germany

Karlsruhe, January 2007

Introduction:

Run-Time and Dynamic Reconfiguration are characterized by the ability of underlying hardware architectures or devices to rapidly alter (on the fly) the functionalities of its components and the interconnection between them to suit the problem. Key to this ability is reconfiguration handling and speed. Though theoretical models and algorithms for them have established reconfiguration as a very powerful computing paradigm, practical considerations make these models difficult to realize. On the other hand, commercially available devices (such as FPGAs and new coarse-/multi-grain devices) appear to have more room for exploiting run-time reconfiguration (RTR). An appropriate mix of the theoretical foundations of dynamic reconfiguration, and practical considerations, including architectures, technologies and tools supporting RTR is essential to fully reveal and exploit the possibilities created by this powerful computing paradigm. RAW 2007 aims to provide a forum for creative and productive interaction between all these disciplines.

Fields of interest:

Author's contributions come from all areas of dynamic and run-time reconfiguration (foundations, algorithms, hardware architectures, devices, systems-on-chip (SoC), technologies, software tools, and applications). The topics of interest include, but are not limited to:

Models & Architectures

- Theoretical Interconnect and Computation Models (R-Mesh, etc.)
- RTR Models and Systems
- RTR Hardware Architectures
- Optical Interconnect Models
- Simulation and Prototyping
- Bounds and Complexity Issues

Algorithms & Applications

- Algorithmic Techniques
- Mapping Parallel Algorithms
- Distributed Systems & Networks
- Fault Tolerance Issues
- Wireless and Mobile Systems
- Automotive Applications
- Infotainment & Multimedia
- Biology Inspired Applications

Design, Technologies & Tools

- Configurable Systems-on-Chip
- Energy Efficiency Issues
- Devices and Circuits
- Reconfiguration Techniques
- High Level Design Methods
- System Support
- Adaptive Runtime Systems
- Organic Computing

Organization:

Workshop Chair: Serge Vernalde, IMEC, Belgium

Program Chair: Jürgen Becker, Universität Karlsruhe (TH), Germany

Steering Chair: Viktor K. Prasanna, University of Southern California, USA

Publicity Chair (USA): Ramachandran Vaidyanathan, Louisiana State University, USA

Publicity Chair (EU, Asia): Reiner Hartenstein, Kaiserslautern University of Technology, Germany

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