Radiation Hardened Coarse-Grain Reconfigurable Architecture for Space Applications

Sajid Baloch[1,2], Tughrul Arslan[1,2], Adrian Stoica[1,3]

[1]School of Electronics & Engineering. University of Edinburgh, King's Buildings, Mayfield Rd, EH9 3JL, UK

[2]Institute for System Level Integration, The Alba Campus, The Alba Centre, Livingston, EH54 7EG, UK)

[3]NASA, Jet Propulsion Laboratory, 4800 Oak Grove Drive, Pasadena, CA 91109, USA

Abstract

Technology trends are such that single event effects (SEE)a*re likely to become even more of a concern for the future. Decreasing feature sizes, lower operating voltage, and higher speeds, all conspire to increase susceptibility to single event upsets (SEU). Upset in avionics is an established concern. Upset at the ground level is becoming a concern for manufacturers of micro-electronics for terrestrial applications. The use of flip-chip packaging and multiple levels of metals further exacerbate the problem. Typical methods of mitigation that either increase the transistor count or reduce IC performance are not acceptable to commercial manufacturers. SOI technology may help in this regard, but is not a magic bullet to end all SEE concerns. We present unique schemes to model and rectify single event disruption in combinatorial and synchronous parts of a reconfigurable architecture. We compare our scheme with different schemes already introduced and results are reported to prove the efficacy of the proposed radiation hardened reconfigurable architecture.*

Introduction

SEEs are caused when highly energetic particles present in the natural space environments (e.g., protons, neutrons, alpha particles or any other heavy ions) strike sensitive regions of a microelectronics circuit. The outcome of the strike depends on many factors, therefore the strike may cause;

i) No observable effect

ii) A transient disruption of circuit operation,

iii) A change in logic state,

iv) Permanent damage to the device or integrated circuit (IC).

Programmable Logic Devices (PLD), and more specifically Field Programmable Gate Arrays (FPGA), are replacing traditional logic circuits by offering the advantages of high integration (small size, low power, and high reliability) without the disadvantages of custom ASICs (high nonrecurring engineering cost and high risk, especially in limited production volume). Static Random Access Memories (SRAM) based FPGAs offer an additional unprecedented advantage. These can be reprogrammed for an unlimited number of times, even in the end-user's system. In these FPGAs, a multitude of latches, also called memory cells or RAM bits, define all logic functions and on-chip interconnects. Such latches are similar to the 6-transistor storage cells used in SRAMs, which has proved to be sensitive to single event upsets caused by high-energy neutrons [16]. The faults have been observed as bit errors in memories. The phenomenon has been observed at both aircraft altitudes and on ground [13][14][15], and is now considered an issue in the dependability of airborne electronics [13].

As the microelectronics industry has advanced, Integrated Circuit (IC) design in general and reconfigurable architectures (FPGAs, reconfigurable System on Chip (SoC) and etc) in particular have experienced dramatic increase in density and speed due to decrease in feature sizes with which these devices are manufactured. The effects of scaling on the single event response of microelectronics are a direct result of the physics of energy loss, charge collection, and upset due to a cosmic ray striking a junction in an IC. The review here is brief and qualitative. When an energetic ion passes through any material it loses energy through interactions with the bound electrons, causing an ionization of the

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material and the formation of a dense track of electron-hole pairs. The rate at which the ion loses energy is the stopping power (dE/dx). The incremental energy dE is usually measured in units of MeV while the material thickness is usually measured as a mass thickness in units

In the presence of electric fields, these electron-hole pairs quickly separate as they drift in opposite directions in the field and are quickly collected by whatever voltage sources are responsible for the field, thus producing a current transient. In bulk CMOS designs, such electric fields are present across every pn-junction in the device. If an ion strikes a junction connected to a signal node, a current transient is subsequently observed on the signal node as the electric fields in the junction and funnel regions separate the electron and hole carriers. The initial prompt current pulse is short lived, lasting in the order of only 100 to 200 picoseconds [16].

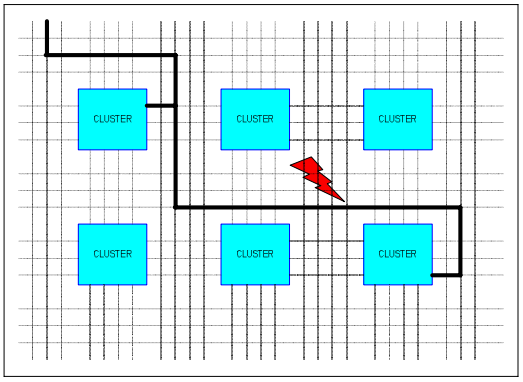

Figure-1 SEU effect on routing-path of a signal

High energy protons and neutrons are also known to produce similar effects indirectly through nuclear reactions within the silicon. In these cases, a heavy ion passes through a junction and produces a similar charge collection current pulse. In space, high energy protons primarily originate from the trapped proton radiation belts and from solar flares. For high-altitude aircraft, both high energy neutrons and protons are encountered as 'reaction by-products', found in cosmic ray showers, formed when an energetic heavy ion from space undergoes a nuclear reaction in the atmosphere [15]. These induced currents are responsible for SEUs observed in space-borne circuits, typically static latches and SRAMs [15]. The effect of these currents on a circuit depends on the response of the circuit to the charge collected on the signal node. Basically, the capacitance of the signal node (to first order) determines how large a voltage swing dV results from the collection of a charge dQ according to of mg/cm^2. The radiation effects community has adopted the term LET (Linear Energy Transfer) for the stopping power. An ion with an LET of 100 MeV-cm^2/mg deposits approximately 1pC of electron-hole pairs along each micron of its track through silicon. dV=dQ/C. For latches and SRAMs, positive gain feedback loops result into a data bit flip once the collected charge reaches a critical value sufficient to drive a node voltage past the switching voltage.

In this paper, we will examine the basic physical mechanisms causing SEE in digital microelectronics for spaceborne applications. Due to reflection of their relative importance in the commercial marketplace, we will concentrate on silicon CMOS devices and digital ICs. Our focus and scope of paper is limited to nondestructive SEEs. We begin with a brief overview of the already proposed coarse grain reconfigurable architecture [1][2] by the authors. Then we will discuss the proposed single-event upset (SEU) mitigation schemes for our reconfigurable architecture. In this paper the mitigation schemes are discussed with particular emphasis on SEU in synchronous and combinatorial elements of the reconfigurable architecture. The traditional SEU mechanism is related to changes in logic state of storage cells (e.g., flip-flops, memories, or latches). We will discuss and show that how the proposed architecture copes with an emerging upset mechanism known as Single-Event transient (SET) that begins to impact on the operation of spaceborne systems when fabricated in deep submicron CMOS and EEPROM technologies. The presented technique addresses both synchronous and combinatorial separately and thus give a simple and a complete solution against radiation induced non-destructive errors (e.g., SEU and SET). The introduced approach not only addresses upsets in latches but also addresses upsets caused by transients in combinatorial logic, global clock signals and global control lines. The novelty of the paper lies in implementing the proposed SEU/SET mitigation techniques [3[4[5] on the reconfigurable fabric to qualify it for mission critical applications. Discrete wavelet transform (DWT) is taken as target application for the proposed architecture. Finally, we conclude with a comparison of the proposed radiation hardened reconfigurable architecture with other different schemes to prove its efficacy.

Reconfigurable Domain-Specific SoC Platform

The authors proposed overall system contains processors and digital Signal Processors (DSP) along-with a number of embedded reconfigurable arrays (RAs) as shown in Figure-2[1][2]. Each RA can be specific to a particular computation such as DWT etc. The system also allows a provision of a combined array that may target multiple computations. The RA can be easily incorporated in to SoC design-flow as a synthesizable soft-core.

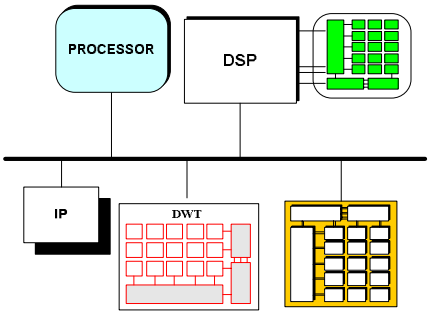

Figure 2: Reconfigurable System-on-Chip [1]

The RA itself consists of programmable clusters which are interconnected through configurable switches [1][2]. The clusters define the functionality of the array. Each RA is heterogeneous and contains different types of clusters, with each cluster specific to one operation. The clusters that constitute the RA can be chosen at design-time according to requirements and constraints. The domain and the degree of flexibility for a RA can be set through the choice of the clusters and interconnects used. The RA is provided as a soft-core which can be simulated, synthesized and routed as a normal ASIC core. This allows RAs to be incorporated into design flow of the full SoC, making the design and verification of the system easier.

In addition, the RA can be configured by a processor or a DSP. This can be done dynamically to allow the adjustment of the RA's operation at run-time. The data from and to the array is read and fed by the processor through an available on-chip bus such as AMBA bus.

The reconfigurable array [1][2] is domain specific and computes the 1-D DWT. The output of DWT array is stored in the main memory and then transposed to be fed into the same RA to get the 2-D DWT output. The reconfigurable array is reused in order to get the 2-D DWT output. Figure-3 illustrates the process. The controller can be a dedicated hardware or can be implemented in software.

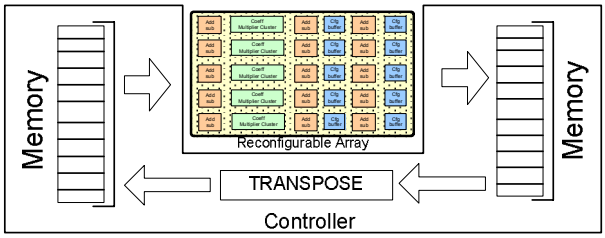

Figure 3: 2-D DWT Mechanism

Reconfigurable Array For DWT

The clusters for the reconfigurable arrays targeting DWT computations were designed for different DWT algorithms including 5/3 and 9/7 with varying performance, speed and area requirements. The following clusters were identified as common reusable blocks and arranged in an array as shown in Figure-4: the clusters are designed with the consideration that the RA can be used fully/partly for any general purpose computations when it is not being used in DWT domain. This feature makes it quite attractive choice for handheld multimedia applications.

A. Add-subtract Cluster

The add-subtract cluster can be configured as:
i) Parallel, digit-serial or bit-serial adder/subtractor
ii) Performs A-B and B-A operation

The basic module is 8-bits wide, three modules are grouped into a cluster and configurable switches are provided between them to support cascading to get wider bit ranges (up to 24-bits). Even wider bit ranges are possible for different operations by cascading multiple clusters through a mesh interconnect.

B. Coefficient Multiplier Cluster

Filter coefficients within the DWT[6][7] computations are multiplied through reconfigurable coefficient multiplier clusters. The floating point coefficients (for 9/7 lifting based DWT) are implemented through canonical-signed-digit (CSD) form [8]. A cluster has programmable shifter blocks, adder blocks and a multiplexer to accommodate a wide range of coefficients. The cluster can handle up to 24-bit operation to facilitate required precision.

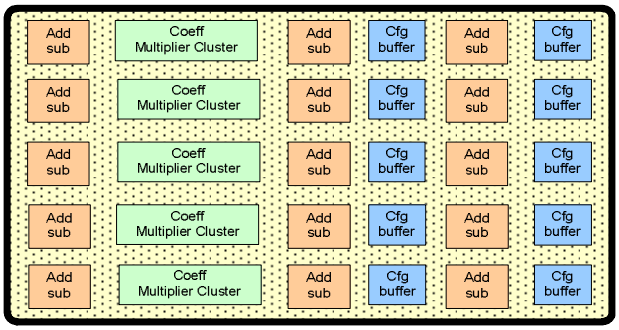

Figure 4: Reconfigurable Array with Cluster for DWT Computations.

C. Configurable Buffer Cluster

The cluster can be programmed for different bit-widths. It has normalizing functionality as well which can be configured depending upon the DWT filter type.

The elements of the array are interconnected through symmetrical configurable switches. Sixteen 4-bit tracks and sixteen-1bit tracks are provided for both data and control lines. Connection boxes (C-Boxes) connect the pins of the cluster to the tracks, and the switch boxes (S-Boxes) connect together the intersection of the tracks [9]. The connection of clusters with tracks is illustrated in Figure-5. The different clusters are arranged in the array to keep the configuration bits and channel track width minimum while maintaining the flexibility of the proposed reconfigurable architecture.

The RA has been specially tailored in terms of size due to the enhanced functionality of the clusters. This helps in reducing the overall power consumption of the improved customized domain-specific array [1][2]. The choice of different cluster's position in the array is inspired by the study of different DWT algorithms and their implementations, for example normalization factor or previously calculated value is required at the end of one calculation cycle and that's a why configuration buffer is placed at the end of each row of the array (Figure-3). Addition/subtraction operations are required frequently in computations and due to this fact the cluster is distributed all over the array.

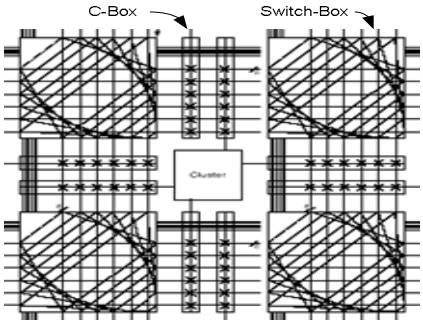

Figure-5 Cluster with S-Boxes and C-Boxes

SEU/SET Elimination For Synchronous Circuit Elements

This section deals with synchronous elements of circuits. The next section rectifies radiation based non destructive faults in the combinatorial logic part of circuits. The authors proposed a technique [3] based on 'Temporal Data Sampling' for synchronous parts of the circuits. A simple embodiment of the Temporal Data Sampling is shown in the Figure-6.

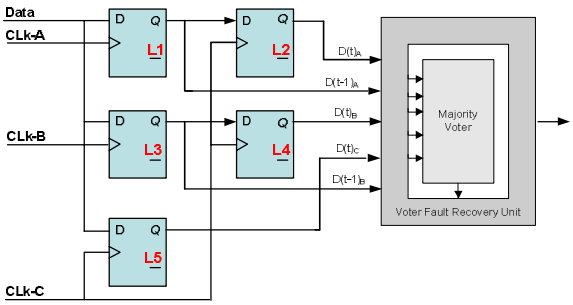

Figure-6: Proposed Temporal Data Sampling [3]

The circuit consists of five 'level-sensitive latches' as shown in Figure-6. Each latch operates in 'Sampling Mode' when its respective clock signal is in high state and in 'Blocking Mode' when clock signal is low. In 'Blocking Mode' the latch holds the data and data changes are blocked. In sampling mode the latch behaves 'transparent' to the incoming data.

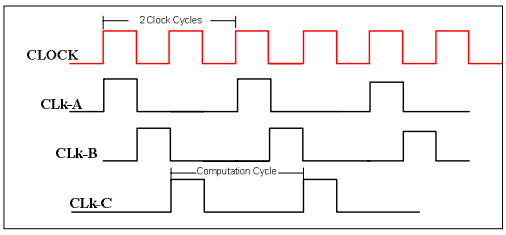

Figure-7: Clocking Scheme for the proposed Architecture [3]

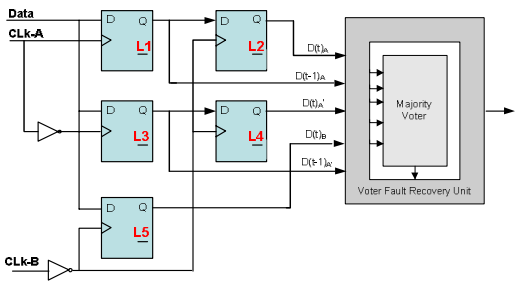

Figure-8: Clocking Scheme for the proposed Architecture [3]

The Temporal Sampling stage helps to store Data samples at different time intervals. These samples are used in voting logic to eliminate single event upsets. Three different clocks (CLk-A, CLk-B & CLk-C) are used. These three clocks have a 90-degree phase shift and 25% duty cycle to cope with the SETs. Figure-7 presents clocking scheme for the proposed mitigation scheme.

Figure-8 shows optimization in the proposed technique. Only two clock signals are used ie. Clk-A and Clk-B. Two data samples are captured on rising and falling edges of Clk-A. The third data sample is captured at falling edge of Clk-B while previously captured data samples are released at the same instance.

SEU/SET Mitigation For Combinational Circuit Elements

The TMR technique is a suitable solution for FPGAs because it provides a full hardware redundancy. However, it comes with some penalties because of its full hardware redundancy, such as area, I/O pads limitation and power dissipation. The amount of reliability required for critical applications such as space is normally accomplished through extra hardware or execution time. It is always necessary to make architectures more reliable with minimum extra components.

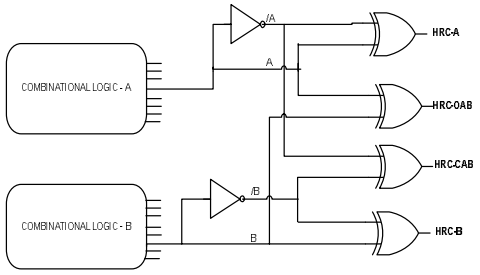

Figure-9: Dual Hardware Redundancy with Comparison [4]

Aiming to reduce the overheads associated with a full hardware redundancy (TMR) and at the same time coping with the transient and permanent upsets, we presented a new technique[4] based on dual hardware redundancy with comparison (DHRC) to detect faults in programmable matrix (SEU in the programmable elements of reconfigurable architecture). The upset detection and voting section are implemented in hardware to eradicate faults and identify fault free block (correct value) to allow continuous operation of circuit. The main objective is to overcome drawbacks of full hardware redundancy (TMR). Moreover, it can present huge area savings for some designs composed of large combinational logic structures.

Figure-11 shows the details of the proposed scheme. As illustrated in the figure-9, there are two redundant blocks: A and B. Four values are captured through auxiliary exclusive OR gates. As a consequence, these four values are used to eliminate the faulty block and help to identify correct the fault free block.

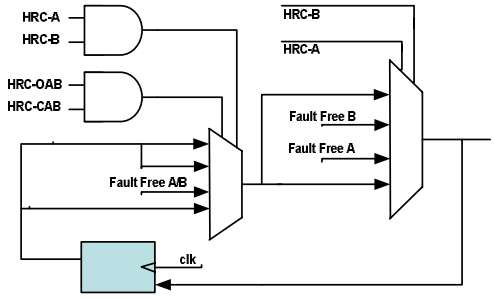

Figure-10: Voter circuit for the proposed scheme [4]

Two samples from each block are used in the proposed scheme: original and complement. HRC-A: hardware redundancy comparator from block A. HRC-OAB: hardware redundancy comparator using original values from block A and B. HRC-B: hardware redundancy comparator from Block-B. HRC-CAB: hardware

redundancy comparator using complemented values from Blocks A and B. Analyzing the sixteen possibilities of output combination of A, /A, B, /B. The voter circuitry is implemented in hardware as shown in Figure-10.

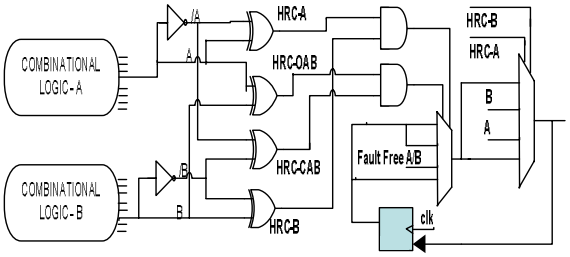

Figure-11: Overall Dual Hardware Redundancy with Comparison [4]

Results

We first elaborate the experimental flow which is incorporated for validating the proposed scheme. Then, we discuss the SEU simulator which we have developed to insert faults representing SEUs. We also discuss the functional testing procedure employed for accessing the SEU immunity of the proposed technique and, then we analyze the results by applying the proposed techniques.

The proposed technique is coded in 'C' programme, which takes Verilog net-list of the circuit under test as input. Verilog net-lists are obtained through Synplify_ASIC 3.0.4 software. D-flip-flops are identified and structural modifications are made to the original circuit by modifying the net-list. The modified net-list is then fed into software simulator to analyze the behavior of the circuit under SEUs/SETs. The SEU immune net-list can be mapped on any ASIC/reconfigurable architecture (FPGA, etc.) through a suitable software tool (Xilinx Foundation Tool, Synplify_ASIC, etc.). A SEU simulator[10] is designed to create a realistic scenario for the faults to be injected into circuit under test due to SEU. The final step is to calculate Error. The circuit under test is introduced with SEU faults through SEU simulator. The functional operation of the proposed technique is compared with the original circuit without SEU faults. A disparity between two circuits indicates that the SEU induced in the circuit has propagated to its outputs, thus leading to a functional failure. The SEU simulator is designed for the purpose of fault injection. The SEU simulator has these three main design considerations. An SEU can occur on any line of the circuit. The fault can flip the logic value at any node. The SEU simulator is designed to randomly inject a SEU fault on any node/signal (0 to 1 or 1 to 0). An SEU can be of variable duration. When an SEU occurs at any node, it inverts the value on that line. The simulator allows the variation of SEU duration. The duration of SEU represents the period of fault injection. An SEU can occur at any instance during the functional operation of application. The SEU introduces a fault on any line at any random time. Figure-12 illustrates operation of SEU simulator.

The Experimental results are derived for ISCAS89 benchmark circuits [11]. These circuits contain combination of synchronous and combinatorial elements. We injected 1000 random SEU, SET faults to verify our proposed scheme. These random fault vectors are stored so that the same faults vectors can be applied to all of the test scenarios which are explained later. Faults were injected through SEU simulator[10]. The proposed reconfigurable architecture can handle all the SEUs and SETs as well and enhances the system performance because no extra hardware/software is required for SETs in the clock. The synthesis tool used for technology mapping and optimization in this paper is Synplify ASIC 3.0.4. The technology used is 0.18 micron Cell library. Post synthesis simulations to verify the proposed technique are performed with the help of Verilog-XL and toggle activity for each node is captured. The power figures are calculated through Synopsis Design Complier with global operating voltage set as 1.8V. There were no power or area figures available in literature for Lima et al. scheme, for the ISCAS89 benchmark circuits. For the sake of a fair comparison, Lima's et al.[12] scheme was implanted on the benckmark circuits and same set of input vectors and random faults are applied.

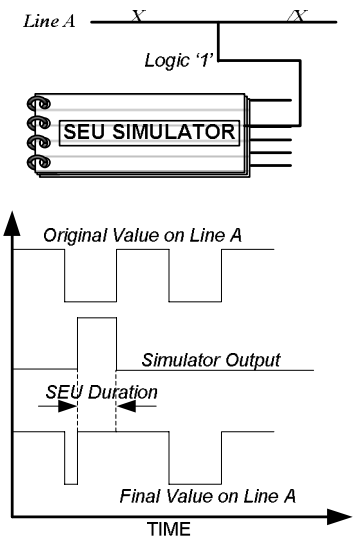

Figure-12: Fault injection process of the designed SEU simulator [10]

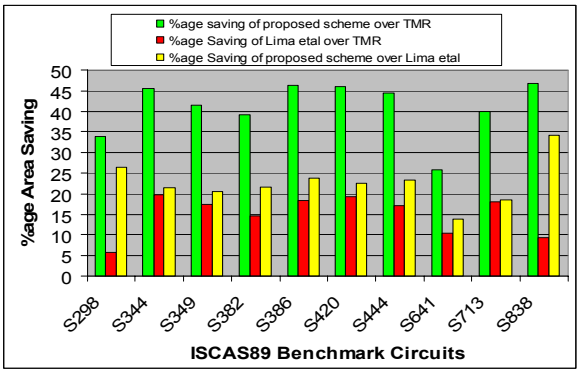

Figure-13: Fault injection process of the designed SEU simulator

The advantage of the proposed scheme over the previous work done by Lima et al [12] is shown in Figure-13 which advocates the efficacy of the proposed scheme over the Lima et.al.[12]. in terms of power consumption. A %age power saving of approximately 37% over lima's scheme is observed. It is vital to compare area overhead because silicon usage has a major impact on performance and cost. Table-2 illustrates the %age area saving of the proposed scheme over different schemes with reference to ISCAS89 benchmark circuits.

	Original	Proposed	PTMR	TMR
9/7DWT	9.8	16.7	20.5	24.9
5/3DWT	4.9	7.98	9.72	13.5

Table-2: Performance Evaluation of the Proposed Architecture – Power Consumption (mW)

The authors then implemented a relative complex computations (5/3 and 9/7 DWT) on the proposed radiation hardened embedded domain reconfigurable array. We implemented the proposed scheme on 5/3 and 9/7 lifting based DWT to advocate its suitability for critical applications. The power consumption(mW) results are reported in Table-2. Different SEU mitigation techniques are compared with the proposed technique along with the probability based scheme (PTMR) proposed by the authors [5].

Circuit	**%age Area Overhead of TMR**	**%age Area Overhead of Proposed Scheme**	**%age Area Over head of Lima et al. [12]**
S298	210%	131%	193%
S344	212%	115%	161%
S349	211%	120%	165%
S382	210%	123%	171%
S386	220%	119%	170%
S420	205%	109%	156%
S444	205%	111%	161%
S641	208%	145%	179%
S713	201%	115%	155%
S838	200%	105%	175%

Table-1: Percentage Area Overhead Evaluation of the Proposed Architecture

The probability based scheme [5] is for combinational circuits and works on input probabilities of gates. The Partial TMR (PTMR) scheme is implemented along with the discussed scheme for synchronous elements. Results are reported in Table-1 for full TMR and for original circuit without any SEU immunity. It is very evident that the proposed scheme is better than the standard TMR and the already proposed probability based scheme by authors [5]. The results are taken at maximum operating frequencies i-e 123MHz.

Conclusion

We have described an SEE mitigation approach that addresses both static latch and transient induced upsets in reconfigurable architectures fabricated in deep submicron technologies and in FPGAs This new approach is based on a concept of sampling data at different time intervals and

presented supporting clocking scheme. Not only are the usual static latch SEUs eliminated, but upsets due to SETs in the combinatorial logic, global clock, and global control signals are also eliminated. The proposed technique can be applied to any general purpose reconfigurable fabric with minimum area and speed penalty. As shown through the results, the proposed coarse grain reconfigurable architecture scheme gives greater power and area savings over schemes already introduced in the literature. The performance edge over other schemes makes the proposed scheme suitable for commercial and military related applications where reliability is a major concern.

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