Power consumption advantage of a Dynamic Optically Reconfigurable Gate Array

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Abstract

Optically reconfigurable gate arrays (ORGAs) are a type of field programmable gate array (FPGA). However, unlike FPGAs, an ORGA can quickly be reconfigured optically using external optical memories and optical connections. Recently, various types of ORGAs have been developed. However, their gate counts were not satisfactory compared with those of FPGAs. Therefore, to improve the gate density of conventional ORGAs, a dynamic ORGA (DORGA) architecture that can remove static memory functions to store a configuration context has been proposed. The DORGA architecture offers not only the advantages of a high gate count, but also the advantage of low reconfiguration power consumption. To date, its power consumption has never been clarified. For that reason, this paper presents measurement results of the optical reconfiguration power consumption of a DORGA-VLSI chip. In addition, the power consumption advantages of the DORGA architecture are clarified through comparison with other ORGAs.

1. Introduction

Recently, high-speed reconfigurable processors and gate arrays have been developed: DAP/DNA chips, DRP chips, and Multi-Context FPGA chips [1]-[6]. Using such programmable devices, only those necessary circuits for a particular task can be downloaded from memory into the reconfigurable processors or into the gate array, thereby increasing the activity of the devices. The internal reconfiguration memory stores reconfiguration contexts of 4–16 banks; then the banks can be changed from one to the other on a clock. Therefore, the ALU of such devices can be reconfigured on every clock cycle in a few nanoseconds. However, increasing the internal reconfiguration memory while maintaining gate density is extremely difficult.

Therefore, optically reconfigurable (programmable) gate arrays (ORGAs) [7]-[11] have been developed to realize both fast reconfiguration and multiple reconfiguration contexts. They can be quickly reconfigured optically using external optical memories and optical connections. However, previously proposed ORGAs require static memory functions to store a configuration context. The static memory function prevents realization of a high-gate-density ORGA.

Therefore, to improve the gate density of conventional ORGAs, a dynamic ORGA (DORGA) architecture has been proposed, [12]-[13], which can perfectly remove static memory function. The DORGA architecture offers advantages of a high gate count along with the advantage of low reconfiguration power consumption which, up to now, has never been clarified. Therefore, this paper shows the measurement results of the optical reconfiguration power consumption of a DORGA-VLSI chip. In addition, the power consumption advantage of the DORGA architecture is clarified through comparison with other ORGAs.

2. DORGA Architecture

2.1. Overview of ORGAs

An overview of ORGAs is shown in Fig. 1. An ORGA consists of a holographic memory, vertical cavity surface emitting lasers (VCSELs), and a gate array-VLSI. Newly available ORGAs[7, 8, 9] can store 100 reconfiguration contexts in a holographic memory. One VCSEL corresponds to one reconfiguration context and is used for addressing the reconfiguration contexts. For example, lighting up one VCSEL, the light propagates to a holographic memory through a free space; then a two-dimensional diffraction pattern is generated from the holographic memory. Finally, a gate array VLSI can receive the two-dimensional diffraction pattern using a photodiode array that is arranged

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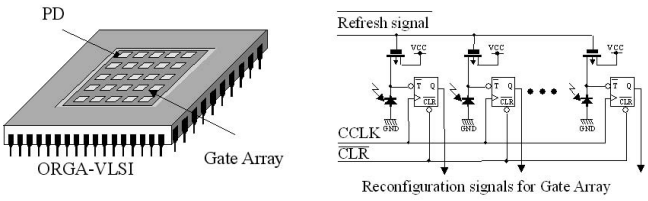

Figure 1. Overview of an ORGA-VLSI and a array of reconfiguration circuits with a static memory fucntion to store a reconfiguration context.

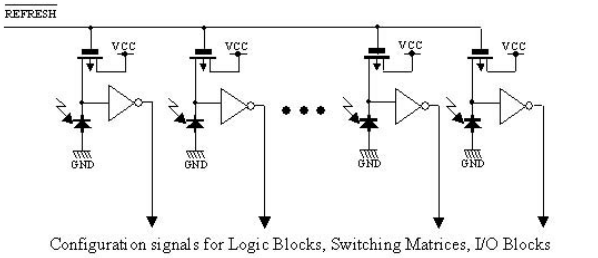

Figure 2. Schematic diagram of an array of dynamic reconfiguration circuits eliminating a static memory function.

in two-dimensions as a reconfiguration context. The architecture allows reconfiguration at over 1 GMHz.

2.2. Previously proposed ORGAs

The VLSI part of previously proposed ORGAs consists of a gate array that resembles those of FPGAs, along with reconfiguration circuits, which include many programming elements. Fig. 1 shows that each programming element requires a photodiode to detect optical reconfiguration contexts, a latch, a flip-flop, or single-bit memory to temporarily store the reconfiguration context. In a previously proposed ORGA, even though the optical memory stores all contexts, the gate array of an ORGA-VLSI maintains one context constantly using a static memory function, as well as FPGAs. However, it can be considered that conventional ORGAs have an excess function because memory functions exist on both sides of the optical part and the VLSI part. In ORGAs, because any configuration context can be programmed quickly from an optical memory to a gate array at any time with little overhead, no static memory function is required on a VLSI part. Even a temporary memory function is sufficient.

2.3. Dynamic ORGA (DORGA)

In dynamic ORGAs (DORGAs), static memory functions to store reconfiguration contexts are eliminated. Instead of latches, flip-flops, or memory, the gate array information is stored in the junction capacitances of photodiodes. A schematic diagram of an array of dynamic reconfiguration circuits is depicted in Fig. 2. Therefore, the reconfiguration circuit of DORGA comprises merely refresh transistors, photodiodes, and inverters. This approach provides an implementation area advantage along with a power consumption advantage. The following describes the power consumption advantage over other ORGAs.

3. Power Consumption Estimation

In DORGAs, along with reducing the implementation area, the total power consumption can also be reduced dramatically. In this section, the common power consumption estimation that is applicable for any ORGA is shown. The power consumption of the ORGA consists mainly of laser, photodiode, and static memory functions' aggregate power consumption. Using the power consumption P_{PD} of charge-integrated photocircuits, power consumption P_{Laser} of laser light sources, and power consumption P_{Memory} of static memory function, the following equation describes necessary total power $P_{Configuration}$ to supply the laser, the charge integrated photocircuit, and the memory function:

$$P_{Configuration} = P_{Laser} + P_{PD} + P_{Memory}\,. \tag{1}$$

In the charge-integrated photocircuit, power is consumed to step up the junction capacitor voltage of photodiodes from 0 V to a power supply voltage. Power P_{PD} is given as

$$P_{PD} = \kappa n C_J V^2 f_c\,, \tag{2}$$

where C_J is the junction capacitance of a photodiode including the load capacitance of the first inverter of the photodiode. Also in that that equation, V is power supply voltage, f_c is the reconfiguration frequency, n is the number of photocircuits, and κ is the switching activity of the photocircuit, which is defined as the expected number of irradiations during one clock cycle. On the other hand, the power to supply the laser is calculated using the efficiency η_L of a laser, diffraction efficiency η_D of optical components, and quantum efficiency η_Q of a photodiode, as

$$P_{Laser} = \frac{\kappa n}{\eta_Q \eta_D \eta_L} \frac{h\nu}{e} C_J V f_c\,, \tag{3}$$

where h, e and ν respectively indicate Planck's constant, electron charge, and laser light frequency. The equation,

which is expressed in a time-independent form, shows the necessary power to discharge the electric charge stored in the junction capacitor of the photodiode. In addition, the power consumption of memory functions is defined as follows:

$$P_{Memory} = \kappa n C_m V^2 f_c \,, \tag{4}$$

where C_m shows load corresponded to be changed the state of memory function. Eqs. (2), (3) and (4) are substituted into Eq. (1) as

$$P_{Configuration} = \kappa n V^2 f_c (C_J + C_m + \frac{C_J}{\eta_Q \eta_D \eta_L} \frac{h\nu}{eV}) \,, \tag{5}$$

where DORGA takes $C_m = 0$, and the other conventional ORGAs take $C_m \neq 0$.

4. ORGA-VLSIs specifications

To estimate the power consumption difference between the DORGA architecture and another architecture with static memory function in the reconfiguration procedure, a DORGA-VLSI chip and a flip-flop type ORGA-VLSI chip with identical technology, the same gate array, the same photodiodes, and the same design method were prepared. Both ORGA-VLSI chips were designed using 0.35 μm standard CMOS processes. The voltages of core and I/O cells were designed identically with 3.3 V. Photodiode and photodiode cell sizes including a refresh transistor and an inverter are respectively 25.5 $\mu m \times$ 25.5 μm and 40.5 $\mu m \times$ 33.0 μm. The photodiodes were constructed between the N-well and P-substrate. The photodiode cells are arranged at 99 μm intervals in two dimensions. The total number of photodiodes is 605. In the flip-flop type ORGA, the output of each photodiode cell is connected to a flip-flop as the static memory function. The output of the flip-flop is connected to each programming point of the gate array; in the DORGA, the output of each photodiode cell is connected directly to each programming point of the gate array. For design, a Synopsys Inc. Design Compiler and Apollo were used, respectively as the logic synthesis tool and the place and route tool. The top metal layer was used for guarding transistors from light irradiation. The other two layers were used for wiring.

The gate arrays of both ORGA-VLSI chips consist of four optically reconfigurable logic blocks (ORLBs), five 4-direction optically reconfigurable switching matrices (4-ORSMs), and optical reconfigurable I/O blocks including four I/O bits (ORIOBs). All routing channels include the same eight wires, which are connected by 4-ORSMs. The gate array functionality is fundamentally identical to that of conventional FPGAs. The ORLB consists of a 4-input look-up table (LUT) and a D-flip-flop (D-FF). The structure of the ORSMs is fundamentally the same as those sold by Xilinx Inc.

5. Experimental Results and Discussions

The power consumption of a DORGA-VLSI and a flip-flop type ORGA-VLSI were measured as 94.1 mW and 100.7 mW, respectively, at a 50 kHz reconfiguration cycle by using a chip board as shown in Fig. 3. The power consumption of a DORGA-VLSI and a flip-flop type ORGA-VLSI were also measured respectively as 191.4 mW and 232.7 mW at 1 MHz reconfiguration cycle. The ratio to DORGA-VLSI and flip-flop type ORGA concurred with those of the theoretical analyses. However, the experimental result includes the power consumption of gate array activity. Therefore, to divide those issues the following discussion is based on theoretical analyses using eq. (5).

Therein, $C_j/\eta_Q = 314fF$ was extracted experimentally; $C_j = 106fF$, $C_m = 202fF$ are calculated theoretically and from HSPICE simulation results. The power consumption of the optical reconfiguration procedure of a flip-flop type ORGA-VLSI part at 100 MHz was 101.5 mW. In addition, at that time, the necessary laser power was calculated as 307.2 mW. As a result, the total optical reconfiguration power consumption was calculated as 408.7 mW at 100 MHz theoretically. On the other hand, the power consumption of the optical reconfiguration procedure of DORGA-VLSI part at 100 MHz was 34.4 mW. At that time, the required laser power was calculated as 307.2 mW, the same as that of the flip-flop type ORGA-VLSI part. Results showed that the total optical reconfiguration power consumption was calculated as 331.6 mW at 100 MHz theoretically.

From the results described above, the reduced power consumption was confirmed as 67.1 mW (Δ 18.9%). The power consumption advantage of the DORGA might be considered as slight from the comparison results. However, a slight advantage arose from prototype chips with large size photodiodes. In the future, we have a plan to reduce the size of photodiodes to 2 um by 2 um, thereby decreasing the power consumption dramatically. Using 2 um by 2 um photodiodes for the DORGA-VLSI chip, the power consumption will be reduced to 3.4 mW, whereas the power consumption reduction of the flip-flop type ORGAs will be limited to 69.4 mW. At that time, the power consumption of the DORGA will be reduced by less than 5% compare with that of flip-flop type ORGAs. We could conclude that, in DORGA architecture, in addition to gate-count advantages, the power consumption advantage is also extremely large.

$\kappa = 1/2$	; Switching Activity
$n = 605$	; Number of programming elements
$\eta_L = 0.2$	; Laser Efficiency
$\eta_D = 1$	; Diffraction Efficiency
$\eta_Q < 1$	; Quantum Efficiency
$\nu = C/\lambda (= 850nm)$	; Laser Light Frequency
	; C = Light velocity in a vacuum
	; λ=Wave length
$V = 3.3[V]$	; Power Supply Voltage
$f_c = 50[kHz]$	; Reconfiguration Frequency

Table 1. Parameter Definition.

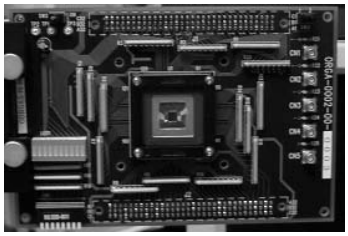

Figure 3. Chip board photograph.

6. Conclusion

This paper has presented measurement results of the optical reconfiguration power consumption of a DORGA-VLSI chip and flip-flop type ORGAs for comparison with DORGA-VLSI.

The reduced power consumption by changing from a flip-flop type ORGA architecture to a DORGA architecture was confirmed as 67.1 mW (Δ 18.9%). However, a slight advantage resulted from these prototype chips, with their large size photodiodes. In the future, we plan to reduce the size of photodiodes to 2 um by 2 um. By reducing the photodiode size, and by using 2 um by 2 um photodiodes for DORGA-VLSI chip, the power consumption is reduced 3.4 mW, whereas the power consumption reduction of flip-flop type ORGA will be limited to 69.4 mW. At that time, the power consumption of DORGAs will be reduced to less than 5% of that of flip-flop type ORGAs. We conclude that, in DORGA architecture, in addition to gate count advantage, the power consumption advantage is also extremely large.

7. Acknowledgment

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