Increasing Analog Programmability in SoCs

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***Abstract*—The use of programmability in Systems-on-Chip (SoC) brings as the main advantage the possibility of reducing the time-to-market and the cost of design, specially when different systems and functions must cover different markets, going from low-power and low-frequency instrumentation to high frequency communication. This paper presents a technique that can be used to increase the analog programmability in a SoC, also allowing one to integrate more analog functions, while guaranteeing the use of the analog part in a larger range of applications. Practical results are presented showing that the proposed technique can be used from DC to RF applications.**

I. INTRODUCTION

The possibility of integration of a whole system containing analog, digital and even mechanical parts in a single die (see Fig. 1), makes the use of the System-on-Chip (SoC) [1] a common choice for most applications, which range from biomedical instrumentation to radio-frequency communication, for example.

Originally conceived to aggregate a large number of different cores, current days SOCs have such variety of cores inside that, today, one of the main points of research is how one can use this miscellaneous blocks to implement the desired application, without taking too much design time, and with a minimum cost for the project. Some of these techniques, such as Network-on-Chip (NoC), IP reuse and reconfigurability, are already a reality. Our main goal in this work is the use of reconfigurability, which has been widely used in digital designs through the use of FPGAs (Field Programmable Gate Arrays) [2], but still remains out of the main stream in the analog domain. Some of the reasons that preclude the use of programmable analog devices are the huge area occupied by the analog components, and their poor frequency behavior caused by programmability itself.

In this context, this work proposes a low power interface to cope with these frequency limitations in Field Programmable Analog Arrays (FPAAs). We show by experimental results that we can effectively expand the frequency range of commercial FPAAs at a very low cost.

Section II reviews programmability in SOCs. Section III presents the proposed technique to cope with these problems, showing that with the use of a simple frequency-shift interface, the analog programmability can be much more exploited. Finally, section IV shows some practical results that validate the proposed technique.

II. PROGRAMMABILITY IN SOC

The rapid evolution on silicon technologies has brought exponential benefits in cost, integration scale and speed of the systems. However, designs have not closely followed the development of these new technologies, although enhancements on the productivity of the designers have taken place through the years. Recently, it has been proposed the use of reconfigurability, what could guarantee a decreasing in both time-to-market and cost of project in SoC devices [3], [4].

In the digital domain, the FPGA, whose complexity and level of integration become larger by closely following Moore's law, guarantees the desired programmability, allowing one to implement almost any kind of digital circuit. On the other hand, for the analog domain, there is still a lack of analog programmable devices that are able to implement most of the main analog functions. The FPAA (Field Programmable Analog Array) [5], which could be a good alternative to implement such functions, still suffer of two great limitations: area and bandwidth.

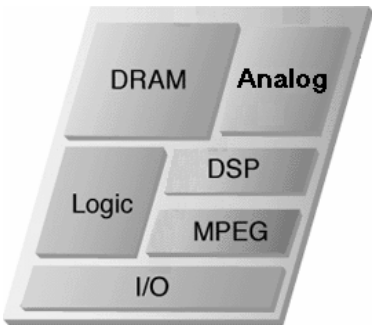

Figure 1. Structure of a SoC containig analog and digital parts.

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FPAA are constituted by a set of configurable analog blocks (CAB), an interconnection network that links these cells and a set of switches used to configure the CAB [5]. In high frequencies, the switches for configuration and those of the interconnection network represent a problem, since parasitic poles are introduced in the signal path. In low frequencies, there is another problem caused by the area occupied by the passive components, mainly capacitors. For example, if one wants to implement a filter using a Gm-C technique, with a transconductance value of 4μS (what represents a resistance of 250KΩ) and a cut-off frequency of 1MHz, the desired capacitor should be in the order of 0.6pF. However, for a cut-off frequency of 1KHz, the value of the capacitor grows to 600pF, taking a large area to be implemented in current VLSI processes.

Today, there are three major vendors of FPAAs. Anadigm produces six FPAAs: the AN10E40 (20 CAB) and those of the AnadigmVortex family, the AN221E02 (2 CAB), AN120E04, AN121E04, AN220E04 and AN221E04, all with 4 CAB. Lattice Semiconductor Corp. produces the ispPAC family, composed by the ispPAC10, ispPAC20, ispPAC30, ispPAC80, ispPAC81, ispPACPOWR604 and ispPAC1208. Finally, Zetex Semiconductors develops the TRAC, also composed by 20 CAB. All of these have some frequency limitation, mainly in high frequencies.

III. PROPOSED TECHNIQUE

Commercial FPAAs have two serious limitations: in low frequency, the use of analog components become limited due to the huge area occupied and in high frequency, the use of switches for programmability limits the frequency of operation, due to the introduction of parasitic poles.

The main question is how to use these limited devices to achieve the implementation of circuits ranging from DC to RF. In this work what is proposed is the use of a generic FPAA, whose band is limited both in low frequencies and in high frequencies, such as the one showed in Fig. 2. This way, a lower analog area can be used, also allowing to integrate more analog components, and the level of programmability is not degraded, since the number of switches is no more a limiting factor. That is, the FPAA is specially designed to work in a specific frequency.

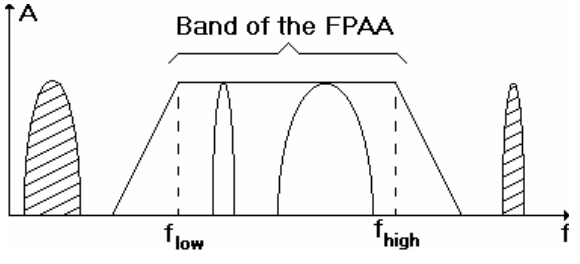

Figure 2. Limited band of a generic FPAA designed to acquire high level of programmability and low area.

For this FPAA, any signal inside its band can be processed through the use of different analog functions (amplifier, filter, comparator, ADC, DAC, rectifier, etc). However, one must still cope with those signals whose frequencies are lower or higher than the frequency of operation of the FPAA, i.e., how can one process the out-of-band signals?

In order to be processed by the FPAA, the out-of-band signals must be moved inside the band of the FPAA, what can easily be done through the use of a mixer and a band-pass filter. Widely used in radios systems, oscilloscopes and TV sets, the mixers are specialized modulators used to shift a signal to a desired frequency [6]. Once the signal is translated, it has to be selected by a band-pass filter, since the mixing process generates more than one component of the signal [7].

Fig. 3 shows how the proposed technique operates. While for the signals below and above the band of the FPAA the interface must up convert or down convert them, for those signals that are already inside this band, a simple bypass switch is used. Fig. 4 shows the structure of the interface, which consists of a mixer whose switching frequency can be easily generated and controlled by a small digital part, and an active band pass filter, whose parameters (cut-off frequency, gain and quality factor) can also be programmable by the same digital block.

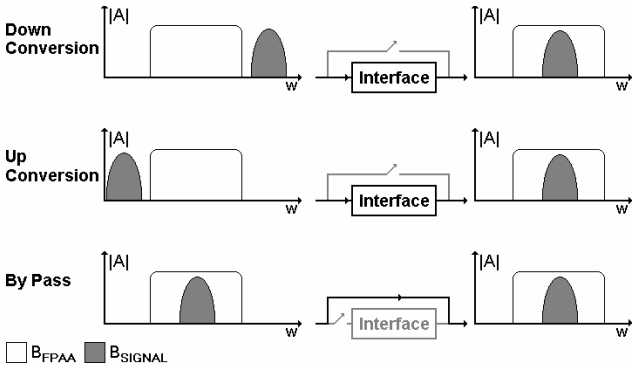

Figure 3. Operation of the proposed interface to move signals inside the band of operation of the FPAA.

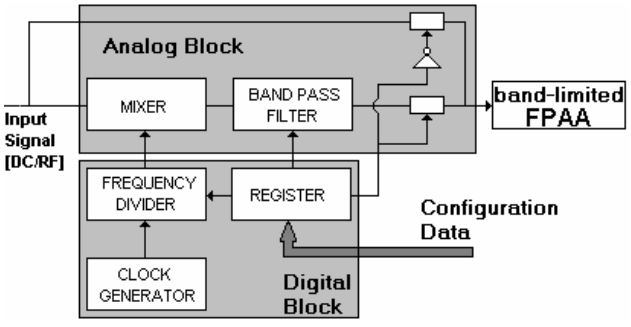

Figure 4. Structure of the proposed interface, constituted by a mixer, a band pass filter and a digital block.

IV. PRACTICAL RESULTS

Let us suppose that f_{low} and f_{high} of the FPAA of Fig. 2 are, respectively, 40KHz and 540KHz, representing a bandwidth of 500KHz, which is sufficient to process many signals such as audio signal modulated in FM (bandwidth of 75KHz), AM (10KHz) or biomedical instrumentation (maximum of 2KHz).

The lower limit of the band guarantees that analog components will take a reasonable amount of area, as discussed in section II. Actually, some of the commercial FPAAs do have such a limitation in the lower limit of the band, such as Lattice ispPAC80 and ispPAC81, whose minimum cut-off frequencies of the feasible low-pass filters are 50KHz and 10KHz, respectively.

The higher limit of the band is still not a very high frequency, ensuring that there are enough switches that guarantee a FPAA with a high level of programmability. Such is the case of Anadigm AN10E40, whose maximum frequency of operation is 500KHz, and allows one to implement more than 50 different analog functions.

With the proposed interface, it will be shown that it is possible to expand the use of these FPAAs, with a small increase of area and power. These circuits could then be used in a SOC analog front-end, with great flexibility.

In the first experiment we show the processing of a signal that is below the lower frequency of operation of the FPAA. A DC Wheatstone bridge is used to measure the variation of a resistive sensor, which is represented by a variable resistor whose resistance varies from 10Ω to 100Ω. To ensure the processing of this signal, whose variation can be extremely slow, it is necessary to up convert it inside the band of the FPAA. A frequency of 50KHz is chosen, once it is higher than the lower limit of the band of the FPAA. The whole system using the FPAA and the interface (mixer, band pass filter and local oscillator generator) was implemented using Anadigm AN221E04. Fig. 5 shows the implemented structure. The band pass filter has a quality factor of 50. The gain of the system is 5. Fig. 6 shows a time domain response of the outputs of the FPAA and the difference between these signals, which corresponds to the desired differential voltage between the two outputs of the bridge used to calculate the variation of the sensor resistance. The variation of the differential voltage versus the variation of the resistance of the sensor is showed in Fig. 7.

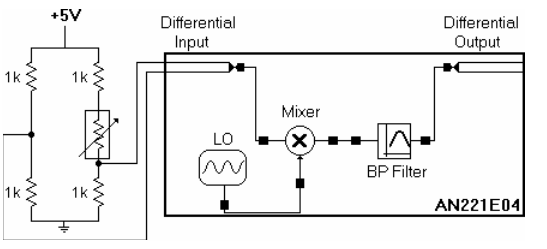

Figure 5. Structure used in the first experiment: Wheatstone bridge plus FPAA.

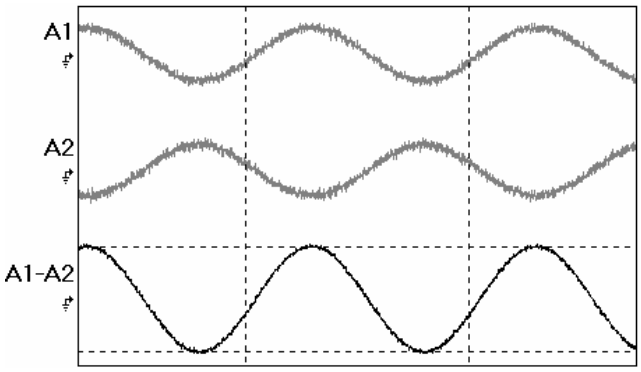

Figure 6. Time domain response of the output of the system.

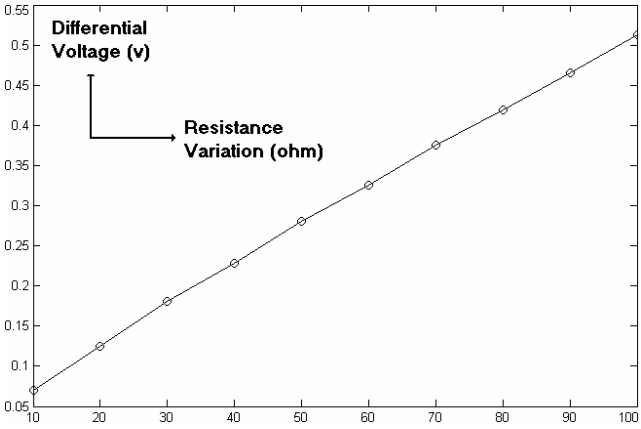

Figure 7. Variation of the differential voltage versus variation of the sensor resistance.

The second experiment shows the processing of a signal that is above the higher frequency of operation of the proposed FPAA. A sequence of AM demodulation (rectifier plus low pass filter) using Anadigm AN221E04 is demonstrated. An amplitude modulated signal with a 1MHz carrier frequency and a 10KHz modulator signal must be demodulated. For this purpose, a down conversion of the signal inside the band of the FPAA must be done. As the FPAA is supposed to have a maximum frequency of operation of 540KHz, the same interface with the programmable mixer was employed to make the down conversion. Fig. 8 shows the complete structure used.

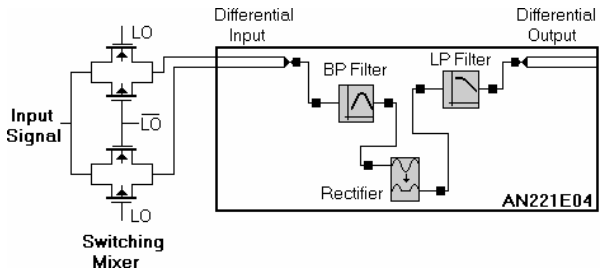

Figure 8. Structure used in the second experiment.

The modulated signal is fed into the switching mixer and down converted to an intermediate frequency of 100KHz and band pass filtered, now by the FPAA that, at this frequency, is able to implement the functions necessary to demodulate the signal.

Fig. 9 shows the acquired input-modulated signal, the down converted signal and the output-demodulated signal.

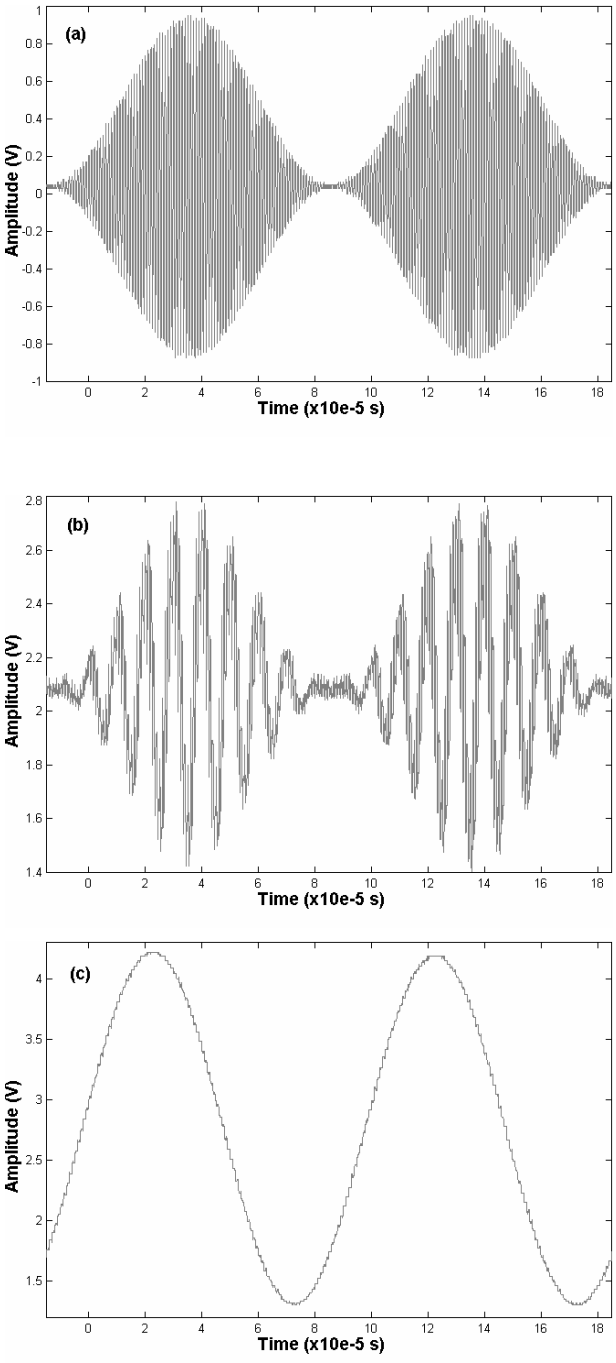

Figure 9. (a) Input AM modulated signal and (b) down converted signal and (c) output-demodulated signal.

V. CONCLUSIONS

A technique to expand the range of applications of the analog blocks of a SoC through the use of reconfigurability is presented. In order to reduce the occupied area and increase the level of programmability, a generic band-limited FPAA is proposed, which uses a programmable frequency-shift interface to allocate the out-of-band signals inside its band. After being processed, the signal can be translated to the original frequency through the use of the same interface.

With the use of such scheme, beyond increasing the range of applications of the analog blocks, a lower power and a lower processing time can be achieved, recovering intrinsic characteristics of high performance analog systems.

Practical results using a commercial device and some discrete components are presented, validating the use of this technique for signals below and above of the minimum/maximum frequency of operation of the FPAA.

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