Interconnect Considerations For High Performance Network on Chip Designs

Uri Cummings
Fulcrum Microsystems

Abstract
Network-on-a-Chip (NoC) is an emerging design style that involves building an on-chip network to link together the logic blocks on a complex system-on-a-chip. The result is any-to-any connectivity for complex data flows and, in early designs, a roughly 3X performance increase over legacy bus-based SoCs. The key design concept in a NoC is replacing the bus with an interconnect switch to link together the autonomous logic blocks. This design is an evolution of the globally asynchronous, locally synchronous (GALS) chip design. This presentation will discuss NoC architecture issues and the use of Fulcrum's Nexus on-chip interconnect technology as the central switching function in these devices.

An elegant solution for this application, Fulcrum's Nexus is a 2.5Tbps non-blocking crossbar with up to 16 independent full-duplex ports, each capable of 160 Gbps of throughput. Nexus is designed using Fulcrum's patented circuit technology that gives the switch an extraordinarily low 3 ns latency, a modest power consumption level that is directly related to activity (300Gb/W) and an ultra small 2 mm x 2mm area.

A Nexus-based GALS architecture provides the foundation for efficiently partitioning the massive amount of transistors available in next-generation, small geometry NoCs. It is estimated that these devices can support as many as two-dozen IP blocks, as compared to 6 or 8 in a typical 130 nm chip design. This will lead to logic blocks separated by very long wires. Locating essential blocks together will mitigate some of these issues, but still many cases will be difficult, such as the processor to I/O connection. In a bus-based SoC design it may take several clock cycles to move data from one end of this massive chip to another– introducing dozens of nanoseconds of latency just for inter-block connectivity. But in a Nexus design, the interconnect is transparent, acting much more like a simple wire than an arbitrated bus with multiple clocked buffers standing between the sending and receiving blocks. The interconnect can receive the data and deliver it instantly to the receiving block for it to consume on its next clock edge – in a few nanoseconds of time.

Nexus also helps to overcome power issues in NoC designs. Fulcrum's unique logic technology is an inherently low power technology, using on average 50 percent less power than traditional globally-timed technology. While each circuit consumes the same amount of power as a traditional circuit when fully operational, when not processing data, each clockless circuit consumes only its leakage current. This results in an average power consumption that rises and falls with ongoing processing. It also means that clock distribution circuitry is not needed.

Nexus-based NoCs also provide a seamless way to bridge the different speeds of each logic block. Nexus' asynchronous nature provides speed-independent ports that allow data to enter into the interconnect at the initiating block's native speed and be switched out of the interconnect at the speed of the receiving logic block with no metastability or rate mismatch issues. As a switch, Nexus can transparently interconnect all of the blocks and transport virtually any type of data (packets, cells, streaming media, etc.). The asynchronous design of the logic block makes Nexus indifferent to varying clock speeds. For high-performance switching applications, and to complement Nexus, Fulcrum has also developed a unique high-performance SRAM technology called RapidArray, which offers exceptionally high throughput for packet storage, and consumes power directly based on activity.

The combination of the two circuits provides the foundation for the high-performance interconnect products that Fulcrum currently offers. The architecture and performance of these NoC devices will be used as examples in the presentation.

Biography
Uri is the Chief Technology Officer at Fulcrum Microsystems. In January 2000, Uri co-founded Fulcrum with Andrew Lines to commercialize their joint research in high performance VLSI design, becoming the founding president and CEO. In April 2001, Uri recruited Bob Nunn, formerly a division GM at Vitesse Semiconductor, to be Fulcrum's President and CEO, and Uri focused on product development. He managed the company's first commercial chip development, a multi-gigabit switch chip, as well as an NRE chip for Intel and numerous other validation chips. He now leads the technology and architecture direction at Fulcrum, and contributes to the roadmap of Fulcrum products. Before Fulcrum, Uri conducted advanced research both in the areas of optical component design and high performance VLSI design. Uri holds 5 issued US Patents from this work. He has a BA Degree in English from Wesleyan University ('94), and a BS ('94), MS ('95), and Ph.D. ('05) Degrees in Electrical Engineering from Caltech. He can be reached at uri@fulcrummicro.com.

1-4244-9707-X/06/$20.00 ©2006 IEEE