Scaling Manufacturability Software to Thousands of Processors

Fabio Angelillis
Synopsis

The main applications in what is called "Design for Manufacturing" (DFM) today are Optical Proximity Correction (OPC) and Fracturing. Both applications modify patterns of an electronic circuit to compensate for manufacturing issues (e.g., lithography, mask writing equipment formats). A leading-edge integrated circuit today has on the order of a billion transistors, which result in the order of a trillion patterns. To be able to process trillions of patterns by complex algorithms in a reasonable time, OPC and Fracturing need to scale to thousands of processors. This talk gives an overview of these problems and explains how they are massively scaled to run on parallel processors.

Biography

Fabio is Vice President of Engineering in the Silicon Engineering Group at Synopsys. He is responsible for industry leading products in the areas of Mask Data Prep, Manufacturing Yield Management, and DFM. He has 22 years of experience in the development and management of R&D organizations across several EDA product lines. He joined Synopsys through its acquisition of Numerical Technologies, where he was Sr. Vice President of R&D. Prior to this role, he worked at Cadence as Vice President of R&D, responsible for some of the most unique and lucrative products in the area of analog and custom design, including Composer, Virtuoso, Analog Artist, Spectre, and physical verification products. In previous years, he held several engineering and management positions at Teradyne and Hewlett Packard. Fabio received his Degree in Computer Engineering from the University of Florida in 1985.

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