An Optimal Simultaneous Diode/Jumper Insertion Algorithm for Antenna Fixing *

Zhe-Wei Jiang[1] and Yao-Wen Chang[2]
[1]Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan
[2]Graduate Institute of Electronics Engineering & Dept. of Electrical Engineering, National Taiwan University, Taiwan
crazying@eda.ee.ntu.edu.tw; ywchang@cc.ee.ntu.edu.tw

ABSTRACT

As technology enters the nanometer territory, the antenna effect plays an important role in determining the yield and reliability of a VLSI circuit. Diode insertion and jumper insertion are the most effective techniques to fix the antenna effect. However, due to the increasing design complexity and the limited routing resource, applying diode or jumper insertion alone cannot achieve a high antenna fixing rate. In this paper, we give a polynomial-time antenna violation detection/fixing algorithm by simultaneous diode/jumper insertion with minimum cost, based on a minimum-cost network-flow formulation. Experimental results show that our algorithm consistently achieves much higher antenna fixing rates than the state-of-the-art jumper insertion and diode insertion algorithms alone.

1. INTRODUCTION

Manufacturing reliability and yield in VLSI designs are becoming a crucial challenge as the feature sizes shrink into the nanometer scale. The antenna effect arising in the plasma process is an important problem in achieving a higher reliability and yield.

1.1 Antenna Effect

The antenna effect is caused by the charges collected on the floating interconnects which are connected to only a gate oxide. During the metallization, long floating interconnects act as temporary capacitors and store charges gained from the energy provided by fabrication steps such as plasma etching, chemical mechanical polishing, etc. If the collected charges exceed a threshold, Fowler-Nordheim (F-N) tunneling current will discharge through the thin oxide and cause gate damage. On the other hand, if the collected charges can be released before exceeding the threshold through a low impedance path, such as a diffusion, the gate damage can be avoided. For example, considering the routing in Figure 1(a), the interconnects are manufactured in the order of poly, metal 1, and metal 2. After manufacturing metal 1 (see Figure 1(b)), the collected charges on the right metal 1 pattern may cause damage to the connected gate oxide. The discharging path is constructed after manufacturing metal 2 (see Figure 1(c)), and thus the charges can be released through the connected diffusion on the left side.

There are three popular solutions proposed to reduce the antenna effect [2]:

1. Jumper insertion: Break the signal wires with antenna violation and route them to the top-metal layer. This approach reduces the collected charges during the manufacturing process, but incurs two vias for each jumper.
2. Embedded protection diode: Add a protection diode on every input port for every standard cell. This approach prevents all input ports from the charge damage, but consumes unnecessary areas when there is no antenna violation at the embedded input port.
3. Diode insertion after routing: Fixing only the wires with antenna violations will not waste routing resources. During wafer manufacturing, all the inserted diodes are floating (or ground). Since the input ports are high impedance, the charge on the wire flows through the inserted floating/ground diode.

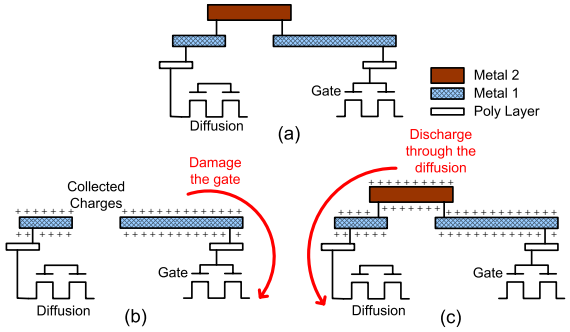

Figure 1: Illustration of antenna effect: (a) An example routing. (b) Late stage of metal 1 layer pattern etching of Figure (a). The collected charges on the right side of the metal 1 pattern may cause damage to the connected gate oxide. (c) Late stage of metal 2 layer pattern etching of Figure (a). All the collected charges can be released through the connected diffusion on the left side.

The difference between diode insertion and jumper insertion is the consumed resources of the fixed circuit. For jumper insertion, each jumper needs free spaces to route to the top-metal layer, and it incurs at least two vias for each jumper. For diode insertion, the consumed resources are the free spaces on the substrate. If a violating wire lies above a space that can insert a diode, the diode is directly inserted below the wire. Otherwise, if there is no free space under the wire, extension wires are necessary to connect the violating wire to a diode insertion space [4]. Both the vias and the extension wires will increase the driving load of the antenna-violating wire, and thus the incurred RC delay will reduce the circuit performance. In current nanometer technology, the induced RC delay of a via is several to tens of times larger than that of $1\mu m$ metal wire. Therefore, in order to minimize the cost of fixing the antenna violations, we shall apply both diode insertion and jumper insertion and consider the interaction between them to minimize the cost for the fixing.

1.2 Previous Work

Maly *et al.* translated the antenna condition detection problem into a layout analysis problem [6]. It can be solved

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by a general-purpose design-rule checking program. However, the method does not indicate any measure to feedback the antenna information to the diode or jumper insertion. Shirota *et al.* proposed a rip-up and reroute method in a traditional router to reduce the antenna effect damage [7, 8]. Ho *et al.* proposed full-chip routing with antenna avoidance [3]. These works [3, 7, 8] reduce the antenna effects during the routing stage while the works presented in [2, 4, 10, 11] try to fix the antenna violations in the post-layout stage. Chen *et al.* presented a heuristic to insert the diode under the wire with antenna violation [2]. However, in modern high-density VLSI circuit, there is little free space for the "under-the-wire" diode insertion. Wu *et al.* in [11] proposed a layer assignment technique to handle antenna avoidance by a tree partitioning algorithm, but routing blockages are not considered in their algorithm. Su and Chang in [9] presented an optimal greedy jumper insertion algorithm that uses the minimum number of jumpers to fix the antenna violation on a spanning tree. Recently, Su *et al.* in [10] further presented a greedy optimal jumper insertion algorithm, called *Bottom Up Jumper Insertion with Obstacles* (BUJIO), which uses the minimum number of jumpers to fix the antenna violation on a Steiner tree with obstacles. Huang *et al.* solved the diode insertion and routing problem by a minimum-cost network-flow based algorithm, called *Diode Insertion and Routing by Min-Cost Flow* (DIRMCF) [4]. The violating wires, the routing grids, and the feasible diode positions are transformed into a flow network, and then the problem is solved by the minimum-cost network-flow algorithm. Both the positions of inserted diodes and the extension wires can be determined through the resulting flow.

1.3 Motivation

In all the previous works [3, 4, 9, 10, 11], the antenna violations are fixed by jumper insertion or diode insertion alone, and the interaction between jumper insertion and diode insertion is ignored. Considering the routing topology in Figure 2(a) and the antenna bound of 5 unit length[1], we need two jumpers for net 1, one jumper for net 2, and two jumpers for net 3 t fix the antenna violation. It requires totally 5 jumpers by jumper insertion alone (see Figure 2(b)) or 7 units of extension wire by diode insertion alone (see Figure 2(c)) to fix the antenna violation. If we consider the interaction between diode and jumper insertion and fix the violations by simultaneous diode and jumper insertion, however, the antenna effects can be fixed by merely one jumper and two units of extension wire (see Figure 2(d)), which consumes much fewer resources than diode or jumper insertion alone.

In [2, 4], one inserted diode is assumed to protect all input ports that are connected to the same output port. This assumption is not always true in real circuits. Such as the tree representation of a given net in Figure 3, both antenna weights (*which could be wire-area-to-gate-size ratios, wire areas, or any other antenna measure*) of segments s_1 and s_2 exceed L_{max}, where L_{max} denotes the upper bound for antenna (i.e., any antenna measure larger than L_{max} will violate the antenna rule). If we insert only a diode on s_1 or s_2, after the metallization of metal layer 1, s_1 and s_2 are still two individual segments, and thus the collected charges on the other segment will still cause damage to the connected input port. That means, in the case of Figure 3, we must insert at least two diodes to fix the antenna violation. Thus, a more accurate algorithm is needed to analyze the number of diodes needed to fix the antenna effect.

1.4 Our Contributions

In this paper, we propose a minimum-cost network-flow based algorithm by simultaneous diode/jumper insertion to aviod/fix antenna violation. The proposed algorithm can find an optimal solution in polynomial time. In particular, it guarantees to fix the antenna violations if one feasible solution exists. We also present a more accurate model to analyze the exact number of diodes needed for antenna fixing. Experimental results show that our work achieves higher antenna fixing rates and incurs lower costs for antenna avoidance/fixing than the state-of-the-art jumper insertion algorithm, BUJIO, and diode insertion algorithm, DIRMCF, alone.

The remainder of this paper is organized as follows. Section 2 formulates the problem of detecting/fixing the antenna effects with simultaneous diode/jumper insertion. Section 3 presents an optimal algorithm for the proposed problem. Section 4 reports the experimental results. Finally, the conclusions are given in Section 5.

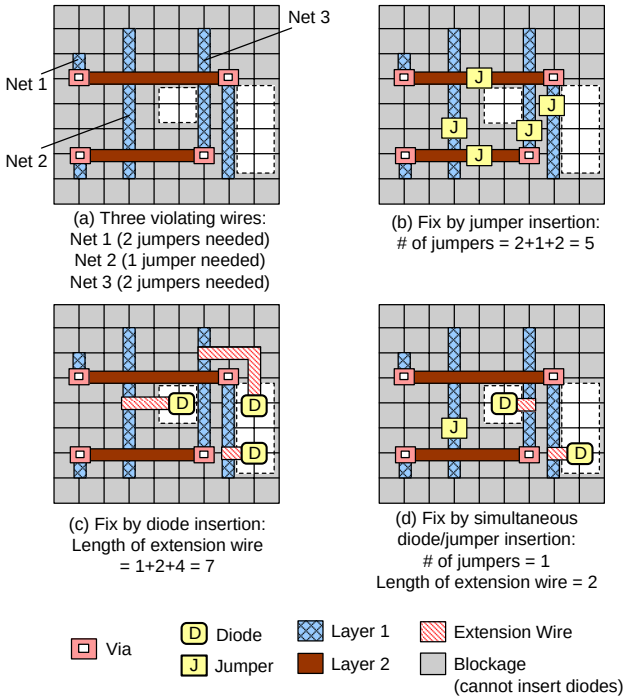

Figure 2: Illustration of the consumed resources by jumpers and extension wires. Three violating wires, nets 1, 2, and 3 need to be fixed.

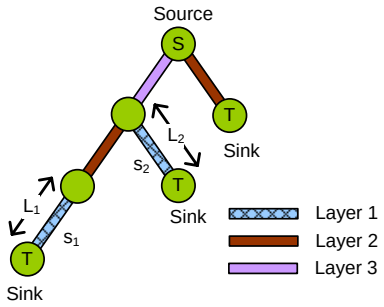

Figure 3: An example that a net needs multiple diodes to fix the antenna violation. If both L_1 and L_2 exceed the antenna threshold L_{max}, at least two diodes must be connected to s_1 and s_2 separately to fix the antenna violation.

2. PROBLEM FORMULATION

To detect/fix antenna violations, we have to check if the effective conductor connecting to a gate oxide exceeds a threshold, L_{max}. Here, L_{max} can be measured in *wire-area-to-gate-size ratio, wire area, wirelength, or any model of the*

[1]Note that the antenna bound could also be measured by wire-area-to-gate-size ratios, wire areas, or any other antenna measure.

strength of antenna effect caused by conductors, same as that in [10]. To simplify the discussion, we assume that all sinks on a net are connected to a gate terminal, while the source is connected to diffusion. (Those sinks connecting to diffusion can be ignored since they will not cause any antenna violation for current technology.) Besides checking the existence of the antenna violation, we have to know where the diodes should be connected to protect the gate terminals. A *violating-wire set* (VWS) is defined as a group of connected wire segments, where exactly one diode needs to be connected to one of these wire segments to fix the antenna violation. Alternately, we can fix a VWS by one or more jumpers instead of one diode. Note that one net can be divided into several VWS's since a net may need multiple diodes to fix the antenna effect, as mentioned in Section 1. Take Figure 3 as an example. The given net contains two VWS's, one contains s_1 and the other s_2. Thus exactly two diodes are needed for the given net.

Vias and metal wires can interplay with each other in many different ways. In this paper, we try to minimize the total delay induced by extra vias and metal wires. To evaluate the total induced delay when we fix the antenna violation, we define the cost function Φ composed of the total wirelength of extension wires (for diodes) and the total number of jumpers as follows:

$$\Phi = \mu \times (\beta \times m_J + l_E), \quad (1)$$

where m_J is the number of jumpers inserted to fix the antenna violations, l_E is the total wirelength of extension wires induced by diode insertion, β is the ratio of the jumper induced delay to the unit-length extension-wire induced delay, and μ is the unit-length extension-wire induced delay. Note that the extension wire does not lie on a signal propagation path since it always connects to a diode. According to the Elmore delay model, only the capacitance of the extension wire is considered and thus the induced delay is linearly proportional to the length of the extension wire. This concept is similar to [4] which minimizes the total wirelength. It should be noted that Equation (1) is merely an example modeling of the interplay of diode and jumper insertion; it will be clear that our algorithm also applies to the cases with different cost models.

With the definitions above, we can formulate the addressed problem as follows:

- **Problem *Antenna Effect Detection/Fixing with Simultaneous Diode/Jumper Insertion* (ASDJI):** Given a routing topology T, an antenna threshold L_{max}, and a set of diode insertion positions D, identify all the antenna violations in T and find a set of feasible jumper positions, a set of diode positions $D' \subset D$, and a set of paths P connecting some VWS's to the corresponding diode positions, such that the total induced cost is minimized, and all the VWS's are either broken into smaller antenna-safe segments by inserted jumpers, or connected to inserted protection diodes.

3. THE ALGORITHMS

We propose a 2-phase method to solve the ASDJI problem. The first phase applies the *Wire Violation Detection (WVD) Algorithm*, and the second uses the *Simultaneous Diode/Jumper Insertion (SDJI) Algorithm*. In the WVD algorithm, all VWS's in the given routing topology are identified, and then in the SDJI algorithm, the identified VWS's are fixed by either diode or jumper insertion with the minimum delay cost. We explain the two algorithms in Section 3.1 and 3.2, respectively.

3.1 Wire Violation Detection

We explain how to identify all the VWS's in this section. In our assumption, the antenna violation happens when the collected charges connected to a gate terminal exceed the antenna threshold during the metallization. Thus, the VWS should be identified by analyzing the intermediate topologies between the metallization of each metal layer. For example, after the metallization of metal layer 2, only segments in metal layers 1 and 2 are fabricated. At this intermediate stage, we should compute the collected charges on the segments in metal layers 1 and 2, and check whether the summation of the collected charges exceeds the antenna threshold. With the nature of metallization, the metal layers are fabricated from the bottom to the top layers. Thus, the proposed algorithm makes use of this nature and analyzes the intermediate topologies between the completeness of each metal layer.

The Wire Violation Detection Algorithm is summarized in Figure 4. The graph G is used to record the intermediate topologies between the metallization of each metal layer, and the set S_{viol} records the identified VWS's. For the main loop in lines 3–10, the segments in each metal layer are added into G in the increasing order of layers. In lines 5–8, since only the collected charges connected to a sink may cause the antenna violation, the connected components which contain at least one sink are extracted from G, and the total antenna weight, W_{Ci}, of each extracted connected component C_i is then computed. If $W_{Ci} > L_{max}$, the collected charges of C_i exceed the antenna threshold and three cases need to be checked (lines 7–8):

- Case 1: C_i is connected to a source node.
  If the connected component C_i is connected to a source node, the collected charges of C_i can be discharged through the diffusion terminal, and thus no antenna violation will occur.

- Case 2: C_i is not connected to any source nodes but is connected to another VWS.
  For this case, if the connected VWS is fixed by diode insertion, the collected charges of C_i can be discharged through the inserted diode, and thus will not cause any antenna violations. However, if the connected VWS is fixed by jumper insertion, the collected charges may still cause the antenna violation, since jumper insertion will not create any discharging paths. In this phase, the case discussed here is treated as antenna-safe segments, and an enhanced technique is applied to solve this case in the second phase.

- Case 3: C_i is not connected to any source nodes or any other VWS's.
  In this case, the collected charges would damage the gate terminals, and thus an antenna violation is identified. The connected component C_i is classified as a VWS and is added into S_{viol}.

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ALGORITHM: WIRE VIOLATION DETECTION (WVD)
    Input: Routing topology (T)
           Antenna upper bound (L_max)
           Number of layers (n_layer)
    Output: Set of identified VWS's (S_viol)
begin
1   Graph G ← ∅;
2   S_viol ← ∅;
3   for layer i ← 1 to n_layer begin
4       add segments in layer i into G;
5       for every connected component C in G which
        contains at least one sink begin
6           W_C ← total weight of C;
7           if W_C > L_max and C is not connected to any
            sources or any other VWS ∈ S_viol then
8               S_viol ← S_viol ∪ C;
9       end
10  end
11  return S_viol;
end
```

Figure 4: The Wire Violation Detection algorithm.

3.2 Simultaneous Diode/Jumper Insertion

In this phase, we fix every VWS identified in the first phase by simultaneous diode/jumper insertion with the minimum cost. Since the optimal jumper insertion solution for a VWS can be computed by the BUJIO algorithm [10], we

make use of the optimal solution of each VWS to minimize the cost induced by antenna fixing.

Inspired by the DIRMCF algorithm [4], we also consider the jumper cost in the flow network, and thus the jumper costs and the extension wire costs (for diodes) can be handled at the same time. For every VWS identified in the first phase, the BUJIO algorithm is applied to compute the number of jumpers, m_J, needed to fix the antenna violation The jumper cost is calculated by $\beta \times m_J$. Then, we add a *jumper edge* for each VWS to model the jumper cost. Consider the example shown in Figure 5 with two VWS's, which are represented by the VWS nodes v_{s1} and v_{s2}. The edges with unit capacity and zero cost are constructed from v_{s1} and v_{s2} to the routing grids, and thus the resulting flow which goes through the routing grids determines the diode positions and the routing of extension wires connected to the protected VWS. Integrating the jumper costs into the flow network, one jumper edge with unit capacity is added from each VWS node to the sink of the network. The costs of the jumper edges are assigned to the optimal jumper costs computed by the BUJIO algorithm. Instead of going through the routing grids, the resulting flow now can alternately go through the jumper edge, which means that lower costs can be achieved if the corresponding VWS is fixed by jumper insertion.

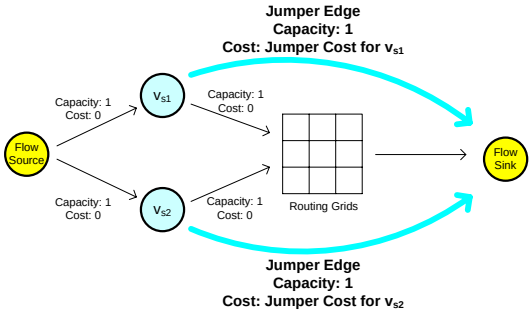

Figure 5: An example to consider diodes and jumpers at the same time. A jumper edge is added for each VWS node, and the jumper cost is modelled as the edge cost.

However, even if the preceding algorithm is applied, some antenna violations may remain in the routing topology. Considering the example shown in Figure 6, the tree representation of a net which contains two identified VWS's. As mentioned in Case 2 of Section 3.1, for a given net N, if at least one of the contained VWS is fixed by diode insertion (see Figure 6(a)), the collected charges of the remainder of N can be discharged through the inserted diodes, and thus no antenna violation remains. In contrast, if all the contained VWS's of N are fixed by jumper insertion (see Figure 6(b)), no discharging path is created, and thus some antenna violation may remain on N if the collected charges of the remainder of N exceed the antenna threshold L_{max}. Through this example, it is obvious that an extra jumper cost, δ_N, is needed for the remainder of N when all the contained VWS's are fixed by jumper insertion. Consider a net N with m identified VWS's. We define $c_J(N)$ as the optimal jumper cost for fixing net N, and $c_J(x)$ as that for fixing a VWS, x. The extra cost δ_N for net N can be computed by $\delta_N = c_J(N) - \left(\sum_{i=1}^{m} c_J(x_i)\right)$.

In the SDJI algorithm, the extra cost δ_N should be added into the fixing cost when all the contained VWS's of net N are fixed by jumper insertion. To achieve this objective, a penalty node, v_p, is constructed for each net. Considering the example shown in Figure 7, the flow network models a net N with $m = 2$ VWS's, represented by v_{s1} and v_{s2}. The jumper edges are connected to v_p instead of the sink of the flow network. Two edges, a *free edge* and a *penalty edge*, are connected from v_p to the sink of the network. For the free edge, the capacity is $m-1$ and the cost is 0. For the penalty edge, the capacity is 1 and the cost is δ_N for net N. With this flow network, if the resulting flow finds fewer than m VWS's to be fixed by jumper insertion, no extra cost will be induced. If the resulting flow finds exactly m VWS's to be fixed by jumper insertion, however, the extra cost δ_N will be induced.

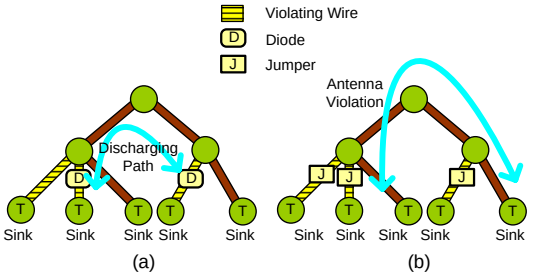

Figure 6: An example to illustrate the interaction between diode and jumper insertion. (a) All VWS's are fixed by diode insertion. The charges on the remainder of the net can be discharged through the inserted diodes. (b) All VWS's are fixed by jumper insertion. The charges on the remainder of the net may still cause the antenna effect.

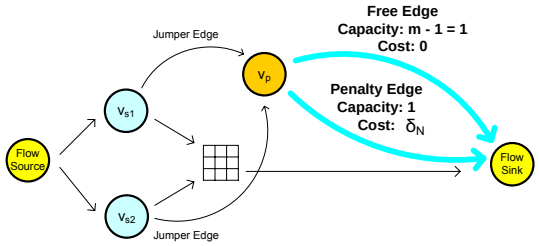

Figure 7: The flow network to handle the extra jumper costs. A penalty node v_p, a free edge, and a penalty edge are added for each net. The extra cost δ_N is modelled as the edge cost of the penalty edge.

3.3 The Overall Design Flow

Given the routing topology T, the antenna threshold L_{max}, and a set of diode insertion positions D, the ASDJI problem can be solved by the design flow summarized in Figure 8. First, for the given T and L_{max}, the VWS's can be identified by the WVD algorithm proposed in Section 3.1. Second, the optimal jumper positions and costs to fix each VWS and the extra costs δ_N for each net N are computed by the BUJIO algorithm. Then, the flow network $G(V, E)$ is constructed as follows:

1. Construct a *flow source*, a *flow sink*, a representing node v_s for each VWS, and a grid node for each routing grid point. The grid nodes can be categorized into three types: v_x represents the grid point occupied by a violating wire; v_d represents the grid point feasible for diode insertion; v_f represents the other grid point not occupied by the routed segments or routing blockages. The capacity of each grid node is equal to 1.

2. For each net containing at least one VWS, construct a penalty node v_p.

3. Construct the grid edges (v_{x_i}, v_{f_j}), (v_{f_i}, v_{f_j}), and (v_{f_i}, v_{d_j}) between neighboring grid points. These edges represent all the possible routing directions of extension wires. All the grid edge capacities equal 1, and all the costs equal the distance between the two grid points.

4. Construct the edges (source, v_{s_i}), (v_{s_i}, v_{s_j}), and $(v_{d_i}$, sink). All the edge capacities equal 1, and all the costs equal 0.

5. Construct the jumper edges from each v_{s_i} to the corresponding v_{p_i} with unit-capacity and corresponding jumper cost. The free edge and the penalty edge from v_{p_i} to the flow sink are constructed as described in Section 3.2.

After constructing the flow network G, the optimal antenna fixing result can be determined by the minimum-cost network-flow algorithm. The diode and jumper positions can be extracted by checking the resulting flows on the edges (v_{s_i}, v_{p_i}) and $(v_{d_i}$, sink). The extension wire routing can be extracted by checking the flows on the grid edges. The antenna fixing result with simultaneous diode/jumper insertion can be concluded in the following theorem:

THEOREM 1. *For a routing topology T with m identified VWS's, if the value of the resulting flow f of the SDJI algorithm is equal to m, all the antenna violations can be fixed with the minimum cost. In contrast, if the value of the resulting flow f is less than m, no feasible solution exists to completely fix the antenna effect in T by simultaneous diode and jumper insertion.*

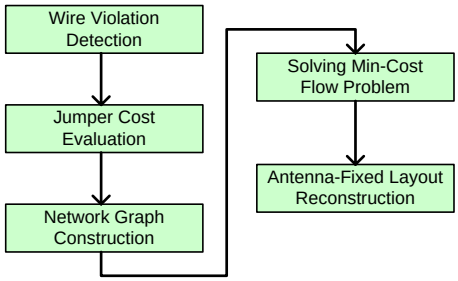

Figure 8: The overall design flow.

The time complexity of the simultaneous diode/jumper insertion (SDJI) algorithm is $O(VE\lg(V^2/E)\lg(V))$, where V denotes the number of grid points and E denotes the number of edges between grid points.

Figure 9 gives an example to illustrate the overall design. We assume that both a jumper and a unit-length extension wire induce one unit delay. Consider the given routing topology with exactly one net in Figure 9(a), and the tree representation in Figure 9(b). Applying the WVD algorithm, two VWS's are identified. By the BUJIO algorithm, each VWS needs one jumper to fix the antenna violation, and thus both the costs of the jumper edges are set to 1. The number of jumpers needed to fix the whole routing tree is 3, and the extra jumper cost δ_N is equal to 1. In Figure 9(c), to construct the flow network, the grid nodes and edges are first extracted from the grid points in layer 1 of Figure 9(a). Then, the jumper edges are constructed for each VWS, and the penalty nodes, the penalty edges, and the free edges are constructed for each net. Since the number of VWS's in the given net is 2, both the capacities of the penalty edge and the free edge are set to 1, and the cost of the penalty edge is set to $\delta_N = 1$. After we construct the flow network, the minimum-cost network-flow algorithm is applied and both the value and the cost of the resulting flow are equal to 2. The optimal fixing solution is finally shown in Figure 9(d).

4. EXPERIMENTAL RESULTS

The proposed algorithm was implemented in the C++ language on a 1.2 GHz SUN Blade 2000 machine with 8 GB memory.

The statistics of the benchmark circuits are listed in Table 1. Six test cases are chosen from the MCNC benchmarks since only these test cases record the source and sink information for each net. The column "Circuit" denotes the circuit name, "Size" denotes the circuit dimension, "# Layers" denotes the number of routing layers, "# Nets" denotes the number of nets, and "# Pins" denotes the number of pins.

The minimum-cost network-flow solver used is LEDA 4.1 [1]. The input routing results of the test cases were taken from the multilevel routing results [5]. According to the

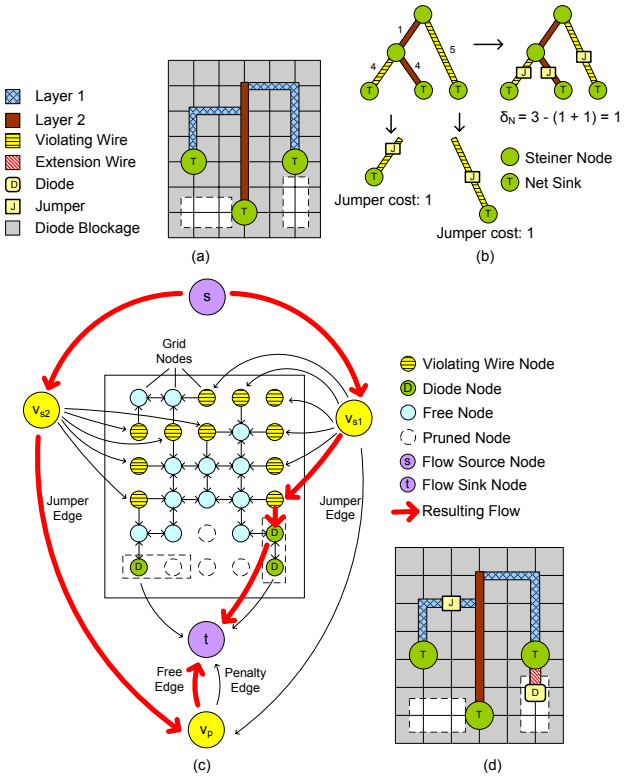

Figure 9: An illustration of the proposed algorithm: (a) The given routing topology. (b) Calculation of the jumper cost for each VWS and the extra jumper penalty. (c) The constructed network graph and the resulting flow. The grid nodes are extracted from the grid points in layer 1 of Figure (a). (d) The resulting layout by simultaneous diode/jumper insertion.

Table 1: The MCNC benchmark statistics.

Circuit	Size (μm^2)	# Layers	# Nets	# Pins
s5378	435×239	3	1693	4818
s9234	404×225	3	1476	4260
s13207	660×365	3	3777	10776
s15850	705×389	3	4470	12793
s38417	1144×619	3	11308	32344
s38584	1295×672	3	14753	42931

TSMC 0.25μm technology file, the jumper-to-wire ratio β in Equation (1) ranges from 10 to 20, and 15 was chosen for all the experiments. The antenna threshold L_{max} set in [3] is 100μm, and in our experiments, 50μm and 100μm were both tested. To reflect modern design complexity, we randomly increase the diode blockage rate of each circuit to 80%, 85%, 90%, and 95%. We compared our work with the jumper insertion algorithm BUJIO [10] and the diode insertion algorithm DIRMCF [4]. We integrated both works with our wire violation detection (WVD) algorithm to identify the antenna VWS's. The experimental results show that our work achieves very high antenna violation fixing rates even in high-density circuits.

Table 2 gives the comparison of the antenna violation fixing rates between BUJIO and our work. Columns 1, 2, and 3 give the circuit name of each test case, the antenna threshold L_{max}, and the numbers of antenna violations, respectively. Columns 4, 6, 8, and 10 give the numbers of fixed antenna violation, and Columns 5, 7, 9, and 11 give the fixing rates of BUJIO and our work in different diode blockage rates. Note that for jumper insertion alone, the diode blockage rate would not influence the fixing result since jumper insertion only consumes the free spaces in the routing layers above the violating wires. The fixing rate is calculated by (# fixed antenna violations)/(# antenna violations). It is

Table 2: Comparison with BUJIO.

Circuit Name	L_{max} (μm)	Total # Viol.	BUJIO [10] # Fixed Viol.	BUJIO [10] Fixing Rate (%)	Our Work Blockage Rate: 80 # Fixed Viol.	Our Work Blockage Rate: 80 Fixing Rate (%)	Our Work Blockage Rate: 85 # Fixed Viol.	Our Work Blockage Rate: 85 Fixing Rate (%)	Our Work Blockage Rate: 90 # Fixed Viol.	Our Work Blockage Rate: 90 Fixing Rate (%)	Our Work Blockage Rate: 95 # Fixed Viol.	Our Work Blockage Rate: 95 Fixing Rate (%)
	50	95	65	68.42	95	100	95	100	95	100	95	100
s5378	100	49	44	89.80	49	100	49	100	49	100	49	100
	50	56	34	60.71	56	100	56	100	56	100	56	100
s9234	100	22	17	77.27	22	100	22	100	22	100	22	100
	50	164	86	52.44	164	100	164	100	164	100	164	100
s13207	100	83	51	61.45	83	100	83	100	83	100	83	100
	50	182	93	51.10	182	100	182	100	182	100	182	100
s15850	100	98	54	55.10	98	100	98	100	98	100	98	100
	50	406	231	56.90	405	99.75	403	99.26	401	98.77	396	97.54
s38417	100	184	122	66.30	184	100	183	99.46	183	99.46	182	98.91
	50	550	341	62.00	550	100	550	100	550	100	550	100
s38584	100	283	167	59.01	283	100	283	100	283	100	283	100
			Avg.	63.38	Avg.	99.98	Avg.	99.89	Avg.	99.85	Avg.	99.69

Table 3: Comparison with DIRMCF for 90% diode blockage rate

Circuit Name	L_{max} (μm)	Total # Viol.	DIRMCF [4] # Fixed Viol.	DIRMCF [4] Fixing Rate (%)	DIRMCF [4] # Diodes	DIRMCF [4] E. Wire Cost (μm)	DIRMCF [4] CPU Time (s)	Our Work # Fixed Viol.	Our Work Fixing Rate (%)	Our Work Jumper Cost	Our Work # Diodes	Our Work E. Wire Cost (μm)	Our Work Total Cost	Our Work CPU Time (s)
	50	95	87	91.58	87	543.6	2.8	95	100	210	81	306.72	516.72	2.1
s5378	100	49	48	97.96	48	266.4	2.2	49	100	60	46	80.64	140.64	2.7
	50	56	52	92.86	52	560.16	2.1	56	100	195	45	290.16	485.16	1.4
s9234	100	22	22	100	22	190.08	0.9	22	100	30	20	63.36	93.36	0.8
	50	164	159	96.95	159	1271.52	33	164	100	465	134	511.2	976.2	28.5
s13207	100	83	82	98.80	82	200.16	11.9	83	100	120	75	83.52	203.52	9.4
	50	182	181	99.45	181	1450.8	76.5	182	100	390	156	617.76	1007.76	56.9
s15850	100	98	98	100	98	175.68	29	98	100	90	92	63.36	153.36	20.8
	50	406	381	93.84	381	4007.52	260.8	401	98.77	1320	316	1870.56	3190.56	265
s38417	100	184	183	99.46	183	543.6	169.1	183	99.46	255	167	231.12	486.12	118.2
	50	550	519	94.36	519	6348.96	320.2	550	100	2040	428	1968.48	4008.48	184.9
s38584	100	283	281	99.29	281	1356.48	102.4	283	100	345	261	408.96	753.96	201.6
			Avg.	97.05				Avg.	99.85					

not surprising that BUJIO achieves only 63.38% fixing rate on average since the routing layouts are usually too dense to find feasible jumper positions. In contrast, our work achieves more than 99.6% fixing rate even with the 95% diode blockage rate.

Table 3 gives the comparison of the antenna-fixing results between DIRMCF and our work. Due to the space limitation, only the detailed results for the 90% diode blockage rate are listed here, and we summarize the results for other diode blockage rates in Table 4. In the table, Column "# diodes" gives the numbers of diodes used to fix the antenna violations, Column "E. Wire Cost" gives the total length of extension wires, and Column "Jumper Cost" gives the jumper cost to fix the antenna violations, which is calculated by $\beta\times$ (number of jumpers used). Column "Total Cost" gives the cost to fix the antenna violations, which is the summation of the jumper cost and the extension wire cost. Note that the total cost in DIRMCF is equal to the extension wire cost. Column "CPU Time" gives the runtime for both algorithms.

As shown in the table, our work completely fixes all antenna violations for all test cases except for "s38417", while DIRMCF cannot for most cases. For those cases with the 100% fixing rate, our work always achieves lower fixing cost than DIRMCF. Table 4 summarizes the average fixing rates of DIRMCF and our work for 80%, 85%, 90%, and 95% diode blockage rates. Column "Fixing Rate 80" gives the average fixing rates with the 80% diode blockage rate, and so on. It is nature that the fixing rate of both works decreases as the diode blockage rate increases since less space is available for diode insertion. The results show that our work consistently achieves very high fixing rates at more than 99.69% even for 95% diode blockage rate while the average fixing rate of DIRMCF decreases to 94.04% at the same blockage rate.

Table 4: Average fixing rate comparison with DIRMCF

Algorithms	Fixing Rate 80	Fixing Rate 85	Fixing Rate 90	Fixing Rate 95
DIRMCF [4]	98.85%	98.45	97.05%	94.04%
Ours	99.98%	99.89	99.85%	99.69%

5. CONCLUSIONS

We have proposed an optimal algorithm to solve the antenna effect detection/fixing with simultaneous diode/jumper insertion problem. Our algorithm guarantees to find the optimal antenna fixing solution with diode/jumper insertion if such a solution exists. Experimental results have shown that our work achieves higher fixing rates and lower delay costs even for high-density circuits compared with the state-of-the-art previous works.

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