Carbon Nanotube Transistor Circuits – Models and Tools for Design and Performance Optimization

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ABSTRACT

In this paper, we describe the development of device models and tools for the design of new transistors such as the carbon nanotube transistor. An HSPICE model for enhancement mode nanotube transistor has been developed. It can be used for design of nanotube transistor circuits as well as to study performance benefits of the new transistor. A model of the carbon nanotube transistor with Schottky barrier is presented. The model enables device design and performance optimization.

1. INTRODUCTION

The principal challenges of the semiconductor industry at the nanoscale are: (1) power and performance optimization, (2) device fabrication and control of variations at the nanoscale, and (3) integration of a diverse set of materials and devices on the same chip [1] [2]. Nanotechnology has been put forward as the key to meeting many of the challenges of the industry. New physical phenomenon and chemical/biological synthesis techniques are being explored. While there have been significant accomplishments in scientific discovery at the nanoscale, the engineering work that is required to harness the science into manufacturable technologies is just beginning.

In this paper, we focus on the use of the carbon nanotube transistor as a logic switch. While very promising experimental results have been published in the past few years, these results are mostly on a single-device level with a focus on scientific discovery. In order to develop a new transistor into a bona fide technology, an engineering approach needs to be adopted. We need to develop the necessary device models and design tools with the appropriate level of abstraction to enable the ***design*** of a useful system. This is distinct from the "science" phase of discovery and explanation of physical phenomena.

We will describe the development of the device models and design tools for carbon nanotube transistors. A model [3] for the Schottky barrier carbon nanotube will be described. We use this model in a mixed-mode simulation environment to estimate the energy-delay tradeoff as a function of device parameters such as the Schottky barrier height. We will also describe the development of an HSPICE model of the carbon nanotube transistor [4]. Using this model, we obtain key information such as the delay variation as a function of the nanotube diameter and the source/drain doping level. The development of tools, such as the ones illustrated in this paper, will be necessary for any proposed new device to become a useful technology.

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2. SPICE MODEL FOR THE CARBON NANOTUBE TRANSISTOR

A complete compact circuit model is illustrated by Fig. 1(b), where C_{GB} is the coupling capacitance between gate and substrate, and C_{xy}/C_{yx} are the trans-capacitance pairs. L_{MS} is the magnetic inductance which is three orders smaller than L_{KS}, the quantum inductance of CNT. The device model is represented by CNT chemical potential, instead of the electrostatic potential. There are four Fermi levels (both input and output Fermi levels for source/drain) for each device due to the quantum contact resistance. A 6-port device model, instead of the conventional 4-port FET model, is generated internally. The two benefits are 1) the quantum contact resistances are automatically taken into account so that no artificial external quantum resistance needs to be added, 2) multiple CNFETs with different quantum resistance can be easily cascaded while maintaining the superposition law required for a linear system.

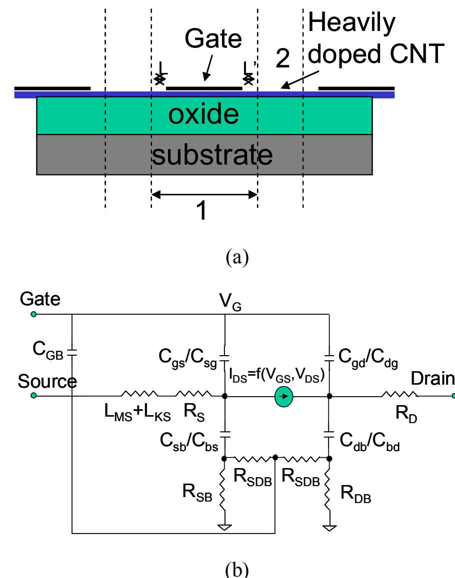

Figure 1. (a) CNFET device layout illustration. (b) Compact circuit model.

The total current contributed by all substates is given by

$$J(V_D,V_G)=\sum_{k_m^{\perp}}\sum_{k_l^{\parallel}}[T_{LR}J_{m,l}(0,\Delta\phi_B)-T_{RL}J_{m,l}(V_D,\Delta\phi_B)]$$

Where $\Delta\Phi_B$ is the CNT surface potential variation, calculated with the charge conservation equation self-consistently

$$C_i[(V_G - V_{FB}) - \frac{(C_i + C_{sub})\Delta\phi_B}{C_i \cdot q}] =$$
$$\frac{2}{L}\sum_{k_m^{\perp}}\sum_{k_l^{\parallel}}\left[\frac{1}{1+e^{(E_{m,l}-\Delta\phi_B)/kT}}+\frac{1}{1+e^{(E_{m,l}-\Delta\phi_B+qV_D)/kT}}\right]$$

C_i is the physical coupling capacitance between gate and CNT channel, and C_{sub} is the physical coupling capacitance between CNT channel and substrate. The first several subbands are doubly degenerated for all chiralities.

This model has been implemented in HSPICE MACRO language. Circuit performance, such as delay, power consumption can be easily obtained. The CNFET circuit performance highly depends on CNT diameter (Fig. 2). Comparison of circuit performance of carbon nanotube transistor and conventional Si CMOS has been made for various benchmark circuits such as NAND, NOR, DFF, and Latch and is described in Deng and Wong [4].

To improve the simulation speed of the carbon nanotube model, the HSPICE subcircuit is rewritten into Verilog-A. While most industrial compact models like BSIMs are written in C, Verilog-A, nevertheless, is chosen in this work due to its many advantages over C in compact modeling [5]. In particular, Verilog-A enables the model to be developed quickly and reliably. It avoids the use of the complicated HSPICE simulator interface and eliminate the calculation of error-prone partial derivatives which are required to be done by hand in C. Verilog-A also has a richer set of algorithms and logic/control functions as compared to HSPICE macros, thereby improving computational efficiency. With the fact that most major commercial simulators support compact models written in Verilog-A, the model also has the advantage that it is portable to other simulators like Spectre. Compared with its HSPICE subcircuit counterpart, the implemented Verilog-A model runs approximately 11 times faster. This dramatic improvement in simulation speed enables us to simulate more complex circuits in a reasonable amount of time.

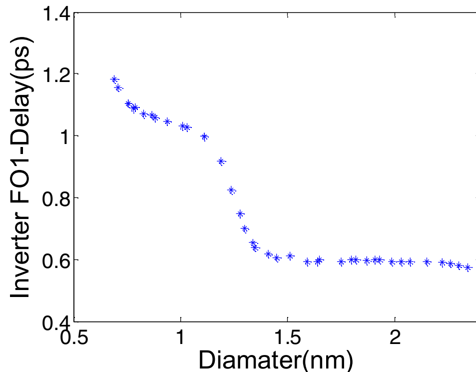

Figure 2. The inverter FO1 delay vs. CNT diameter.

3. SCHOTTKY BARRIER MODEL OF THE NANOTUBE TRANSISTOR

To facilitate device design, a model that reflects the physics of the nanotube transistor in a more accurate fashion is required. We have developed a model of the nanotube transistor including important non-idealities such as the Schottky barrier at the source and drain.

The CNFET structure modeled is depicted in Fig 3. The tube potential at the surface relative to the equilibrium source Fermi level is denoted by μ. Assuming ballistic channel, the $+k_l$ states are filled according to source Fermi level, μ_s and the the $-k_l$ states are filled according to the drain Fermi level, μ_d (l is the direction along tube axis) Poisson's equation in the radial direction requires solving the following equations self-consistently to get the surface potential, μ.

$$V_{gs} = V_{fb} + \mu / q + Q_{cnt} / C_{ins}$$

where V_{gs} is the gate bias, C_{ins} is the insulator capacitance, V_{fb} is the flatband voltage and Q_{CNT} is the charge per unit length in the nanotube

$$Q_{cnt} = q \sum_{k_t} \int_{E_{i\min}}^{E_{i\max}} \frac{1}{2} g_{i,l}(E).(f_s(E,\mu)+f_d(E,\mu))dE$$

where $g_{i,l}(E)$ is the 1D universal nanotube DOS for the ith subband [6]. f_s and f_d are source/drain Fermi-Dirac distribution functions respectively. $E_{i,min}$ and $E_{i,max}$ denote the min/max energy of the ith subband, E_g denotes energy gap for the tube and k_B is the Boltzmann constant.

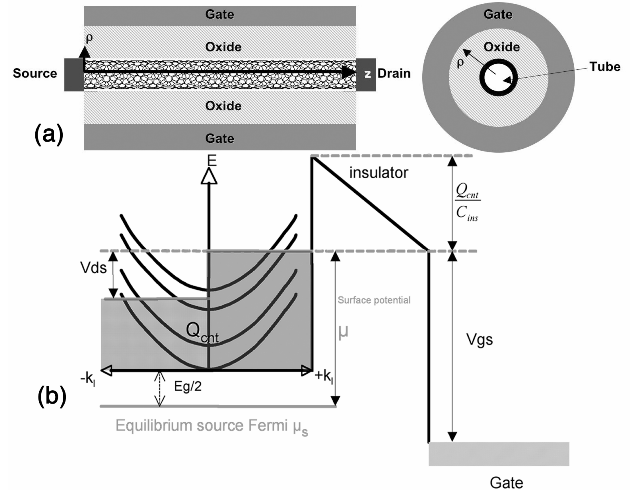

Figure 3. (a) Device geometry cross-sections along the channel direction and normal to the nanotube. Insulator thickness is denoted by t_{ox}, tube length with L and tube diameter with d. (b) Energy profile in ρ direction with superimposed E-k diagram.

The Schottky barriers can be modeled as mesoscopic carrier scattering sites [7]. Carriers, which are initially at thermal equilibrium with the source/drain contacts, are scattered by the SB before entering the channel, where they are no longer at thermal equilibrium. However beyond the energy relaxation length, a pseudo-distribution function can be used to calculate the number of carriers assuming carrier conservation in the scatterer. Let us consider only one "scatterer" near the source end and let the transmission probability across the scatterer at energy E be $T(E)$. From N_s number of carriers at this energy in the source reservoir, $N_s \cdot T(E)$ will make it to the channel. Similarly, from N_d number of carriers injected from the drain contact, $N_d \cdot (1-T(E))$ are reflected from the source scatterer. Thus, from the total number of carriers occupying the $+k_l$ states a fraction of T would have the source reservoir distribution and a fraction of $(1-T)$ would have the drain reservoir distribution, the total distribution would then be

$$f_{+k_l} = T(E).f_s(E) + (1 - T(E)).f_d(E)$$

Similarly if the drain SB is taken into account, the following pseudo-distribution functions can be derived for the $+k_l$ and $-k_l$ states,

$$f^+ = \frac{T_s f_s + T_d f_d - T_s T_d f_d}{1 - (T_s - 1).(T_d - 1)}$$

and

$$f^- = \frac{T_d f_d + T_s f_s - T_s T_d f_s}{1 - (T_s - 1).(T_d - 1)}$$

where $T_{s/d}$ is the transmission probability across source/drain SB. These two new distribution functions have to be used instead of f_s and f_d in presence of the SB. Transmission probabilities are calculated by means of the WKB approximation. The potential profile near the contacts is obtained using the evanescent-mode analysis [8].

Fig. 4 shows I_d-V_{gs} and I_d-V_{ds} plots for similar structures with and without the SB. The drain current is noticeably reduced due to the SB. Fig. 5 shows the effect of the SB height on the ON current. Despite the very short scale length (λ_{CNT}=1~8nm) and the thin SB, the barrier height still affects the ON current. It should be noted, however, since devices exhibit ambipolar characteristics due to the fully symmetric bandstructure for electrons and holes, the mid-gap SB is the worst case.

This ballistic model of the carbon nanotube transistor has been implemented in MATLAB. The computational speed is fast enough to enable a thorough exploration of the device design space to provide guidance for device fabrication and device performance optimization. Issues such as dependence of the device characteristics on device parameter variation (e.g. nanotube diameter variation, gate oxide thickness variation) can easily be studied.

This model can also be utilized in a mixed-mode device/circuit simulation to obtain inverter waveform and inverter delays. Fig. 6 shows one such example.

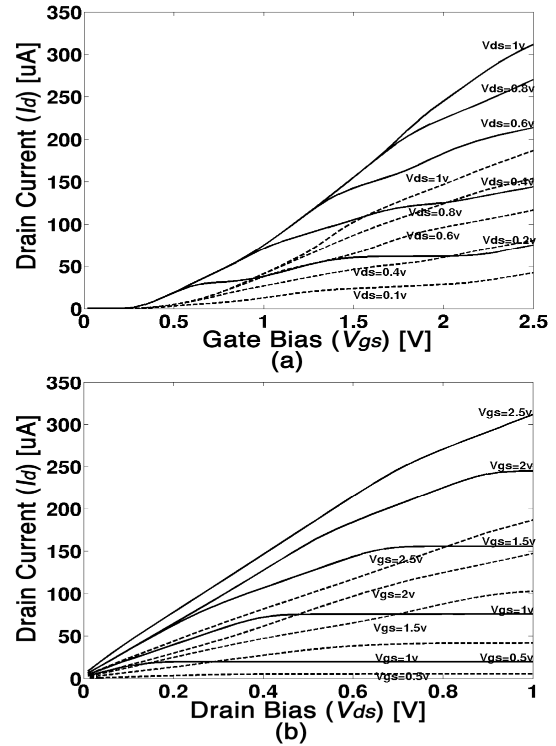

Figure 4. (a) I_d-V_{gs} and (b) I_d-V_{ds} plots for a (19,0) tube, d=1.5nm, t_{ins}=4nm, ε_r=20. ε_0, λ_{cnt}=1.9nm, L=100nm at T=300K. Solid lines are for the no-SB case and dashed lines are for the mid-gap SB case. Note that the drain current saturates slower in the presence of SB.

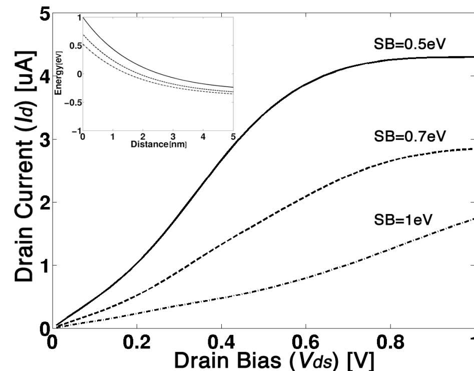

Figure 5. Id-Vds plots for a (10,0) tube, d=0.8nm, tins=4nm, ε=20, λcnt=1.8nm, Eg=1eV, L=100nm. Vgs is 1V. Solid line represents mid-gap SB height (Eg/2). Dashed line is for SB height of 0.7eV. Dashed dotted line is for SB height=1 eV (i.e. contacts aligned to valance band). Note that the current saturates slower for higher a SB height. Inset shows energy diagram near the source region for SB=1eV (solid line), SB=0.7 eV (dashed line) and SB=0.5eV (dash-dotted line). Vds=0.5V in the inset.

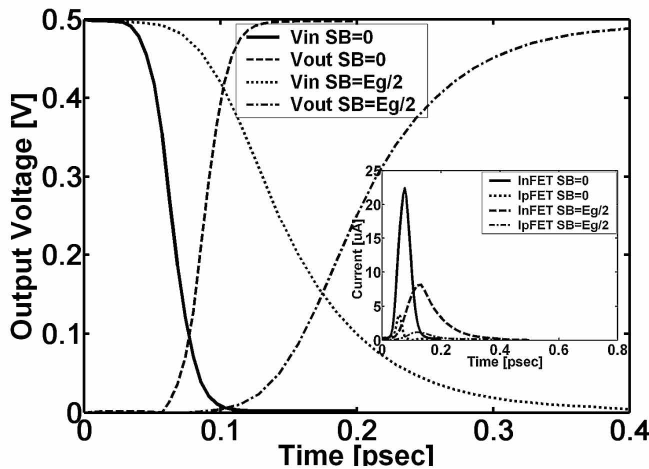

Figure 6. Input and output waveforms for two series inverters. Solid line input to the second gate for SB=0, dashed line output of the second gate for SB=0, dotted line input to the second gate for SB=E_g/2 and dash-dotted line output of the second gate for SB=Eg/2, for the same (19,0) tube of Fig. 3 with L=20nm. Inset shows current for pFET and nFET as a function of time , supply Voltage is 0.5V.

4. CONCLUSIONS

We have described our effort in developing tools for the device design and circuit analysis for new, nano transistors such as the carbon nanotube transistor. Development of these tools is essential for realizing the technology potential of these new devices.

5. ACKNOWLEDGMENTS

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