Prospects for Emerging Nanoelectronics in Mainstream Information Processing Systems

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ABSTRACT
The International Technology Roadmap for Semiconduc-tors (ITRS) seeks to stimulate invention and research lead-ing to one or more new nanoelectronics technologies that may extend functional scaling of information processing substantially beyond "ultimately scaled" CMOS. Introduction of such new technologies is envisioned in two phases – first by extending the CMOS platform via heterogeneous integration of new technologies and, later, via a replace-ment for CMOS that would provide the equivalent of sev-eral more technology nodes beyond ultimate CMOS. 1D charge state materials (nanotubes and nanowires) appear to be particularly attractive for the first phase. Ferromagnetic or spin-based logic devices are under investigation for the second phase. Some recent work in both of these areas will be presented.

Keywords
Nanoelectronics

1. INTRODUCTION
There is a growing consensus within the semiconductor industry that CMOS technology scaling, as currently embodied in the International Technology Roadmap for Semiconductors (ITRS), will reach ultimate limits in the not-too-distant future. The 2005 edition of the ITRS extends out to 14 nm DRAM half-pitch CMOS technology, with physical gate length, Lg of 6 nm, and introduction envisioned for the year 2020. Whether "conventional" CMOS can be ex-tended even further is unclear and a subject of intense re-search. Given the prospect that technology scaling might reach a limit, and thereby fundamentally change the busi-ness model for the entire industry, there is an increasing effort directed towards developing new nanoelectronics technologies that may provide continued functional scaling. A rather comprehensive discussion of the challenges involved and the approaches currently under investigation is contained in the Emerging Research Devices (ERD) section of the 2005 ITRS.

At first, somewhere below about Lg of 15 nm, the MOSFET device structure may change to an advanced, non-classical one such as the FinFET [1]. Later, towards the end of the Roadmap timeframe, the CMOS platform may be enhanced and further extended via heterogeneous integration of new materials and technologies for improved carrier transport such as 1D charge state materials (carbon nanotubes, semi-conducting nanowires) or high mobility semiconductor thin films (III-V compounds or germanium).

Finally, the ERD suggests that the limit of scaling of such a hybrid technology may very closely approach the funda-mental limit for scaling any charge-based switch, and that further improvement in terms of information processing capability with lower power dissipation may require the introduction of alternative logic devices that represent information by state variables other than electronic charge. Such a change would also very likely require the introduction of new, and possibly radically new micro- and nano-architectures.

2. Carbon Nanotube FETs
Carbon nanotubes (CNTs) have attracted considerable at-tention for use as an alternative 1D channel material in an otherwise familiar insulating-gate field-effect transistor (IGFET). Among many 1D materials being investigated currently (including silicon), CNTs show the highest transistor performance so far [2,3], although there are many serious manufacturing issues that remain to be resolved, as discussed in detail in the ERD. Of greatest concern is the fact that when CNTs are grown by any of the currently known methods, their diameter and chirality (a crystallographic property representing the symmetry of arrangement of the carbon atoms in the CNT) are not well controlled. Since these properties in turn determine the band gap and effective mass, a large variation of transistor characteristics results in any collection of CNT FETs. In fact, a significant fraction (10%-40%) of CNTs are metallic and do not show any transistor action. Research is underway to develop growth methods that allow control of diameter and chirality or , in the alternative to separate and purify CNTs by diameter and chirality. However, as pointed out in the ERD, there is currently a lack of a metrology capability to rapidly quantify the bandgap distribution for a large sample of CNTs and this can limit progress in improving growth processes.

We have begun to address this metrology issue, as well as explore the issues involved in monolithically integrating CNT FETs with silicon CMOS technology. We recently demonstrated an integrated circuit combining CNT FET devices with n-channel metal oxide semiconductor (NMOS) field effect transistors. Massive arrays of nanotube devices, each addressed individually

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using the NMOS cir-cuit, were rapidly characterized [4]. More recently [5], we have been able to directly correlate on-current and off-current of CNT FETs with direct atomic force microscopy measurements of the CNT diameter (Fig. 1). The results also show a dependence on the contact metal, indicating that these are Schottky contacts and the barrier height depends on the choice of contact metal. Pd shows the lowest barrier height for these p-type devices.

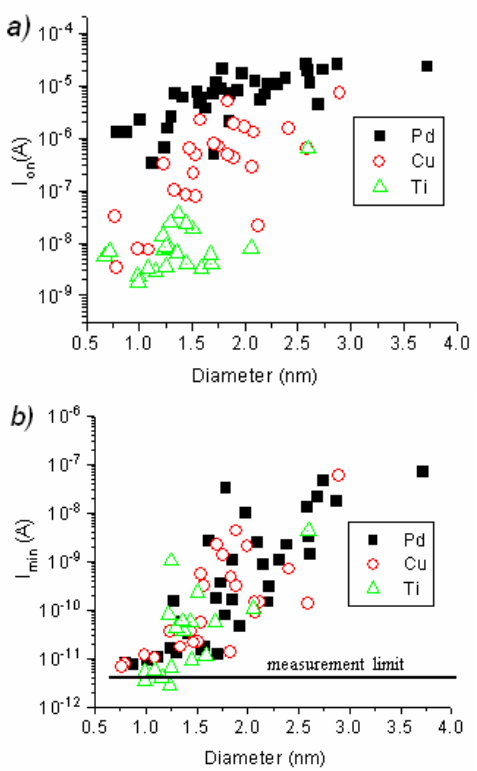

Figure 1. Dependence of on- and off-state current on diameter. a) on-state current vs diameter. b) off-state current vs diameter for the same set of devices. Vd = -2V for Cu and Ti devices. Vd= -3V for Pd devices. (Figure reprinted from Ref. [5])

3. Spintronics

A leading candidate state variable other than charge to be used in alternative logic devices is electron spin (spintron-ics), or the closely related magnetization state of a nano-scale ferromagnet (magnet dot). The recent demonstration of a majority logic gate using ferromagnetic dots [6] has been an important milestone in this area. A closely related field of research is quantum computing, in which ensembles of coherently coupled quantum systems (qubits) are being explored for their potential in performing exponential speed-up in the computation of certain specialized algorithms [7]. We are developing the technology for fabrication of a silicon solid-state quantum computer [8]. Al-though quantum computing has not yet been shown to be capable of general-purpose computing, and solid-state implementations of quantum computing have little hope of operation at temperatures much above absolute zero, many of the component technologies being developed for solid-state quantum computing can be useful for room-temperature realizations of spintronic or magnetic logic, and there is therefore considerable synergy among these fields. For example, our work on spin readout using nanotransistors [8,9] may also be applicable to reading out the output magnetization state of a magnetic logic array as discussed in [6]. We are currently developing such magnetic to electronic interfaces for magnetic logic array systems that can operate at room temperature.

4. Conclusion

In conclusion, all indications at this point in time suggest that conventional CMOS scaling will continue for about another 15 years, and that device innovations such as 1D charge state materials and others may enable continued scaling for a few generations beyond. While that may seem like a long time, there is a great deal of development needed in order bring such novel materials into mainstream high volume manufacturing and there are significant chal-lenges to be overcome.

The prospects for continued increase in the functionality of electronic systems to be provided by improvements in de-vice technology beyond that point are much less clear. Spintronic or magnetic devices show some promise for very low power dissipation, but whether this can be realized in full systems remains to be fully investigated. Also, much work needs to be done to see if these devices can even be scaled to the dimensions of ultimate CMOS, which will be in the range of 6 nm or less. The appropriate logic device that could succeed the CMOS logic gate has probably yet to be invented. This breakthrough will have to be accom-plished and recognized very soon if the technology pro-gression powered by Moore's law style scaling will con-tinue to provide exponential growth of the electronics mar-ket through the decade of 2020 and beyond. Given the time required to introduce and develop this new technology to the scale needed to address that ambitious goal, we may already be behind schedule!

5. ACKNOWLEDGMENTS

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