Near-Term Industrial Perspective of Analog CAD

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ABSTRACT
Analog and mixed-signal CAD looks like a nice success story: there's been significant research in building design automation tools since the late 80's, and commercial tools have been on the market for several years now. However, the majority of AMS (Analog/Mixed-Signal) designers still use manual design only, focused around the SPICE simulator. So why are designers not or slowly adopting these CAD tools? This paper will present a reality check on the current state of the art of AMS design tools for industrial usage.

Categories and Subject Descriptors
B.7.2 [**Integrated Circuits**]: Design aids –*graphics, layout, placement and routing, simulation, verification*

General Terms
Algorithms, Design, Verification.

Keywords
Analog, mixed-signal, integrated circuits, computer-aided design

1. Introduction
Many believe analog circuit design has not changed in 30 years. Is this true? Compared to the digital design revolution, yes; analog design has not changed nearly as much as its digital counterpart. That said, there has been, and will continue to be, evolutionary advancements in analog design automation.

First, let's ask: What does an analog CAD tool need to do to gain industry adoption? The answer is the same with any technological innovation: The value of the tool must be well worth the incremental effort in setting up the design problem. In addition, automated techniques must efficiently solve real design problems, problems that are difficult to solve with manual design techniques. If the manual methodology works, why fix it?
Looking back, advancements in analog design tools have played a critical role in increasing the efficiency of analog circuit design and verification. Going forward, the demand for automated analog design technology will be driven by the challenges of shrinking semiconductors and increasing board and chip speeds.
Let's review a few areas of analog CAD, discuss why certain techniques have been adopted, discuss why others have not, and attempt to forecast which automation techniques will be vital in meeting the near-term future challenges of analog design.

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1.1 The SPICE Advance
Current Status: Starting from roughly the early 1970s, SPICE and SPICE models started to become adopted by analog designers, to their now longtime stature as indispensable design tools. Before SPICE, analog circuit analysis and design was done mostly by hand, by solving equations on paper. SPICE complemented these manual calculations, providing designers with an accurate way to verify their designs, and enabling designers to rapidly understand the effects of process and environmental conditions. SPICE has advanced considerably over the past 30 years. The basic AC, DC, transient and steady-state simulation techniques are much faster and more accurate, and the addition of new analysis techniques has enabled designers to create circuits that operate at high speeds, are tolerant to noise, and have high yield.
The Near Future: Chip and board speeds are increasing. Consequently, advanced signal integrity analysis and models are becoming part of mainstream design. High-speed phase-locked loops are becoming more popular, requiring designers to use RF-styled analysis such as Harmonic Balance to simulate phase noise and jitter effects. As semiconductor device sizes shrink, process variability analyses are becoming increasingly popular with both Integrated Device Manufactures (IDMs) and fabless design houses.

1.2 Fast SPICE and Behavioral Modeling
Current Status: Behavioral modeling has become very popular for testbench development. Designers frequently use the behavioral representations in languages such as Verilog-A, Verilog-AMS and VHDL-AMS to model complex input stimuli. Behavioral models are also used in design when fast turnaround is desirable and rough accuracy is acceptable, such as exploration of system-level architectures. They can be used for bottom-up verification as well, but here they share a usage environment with FastSPICE simulators. Though behavioral models simulate faster, they require designer setup time and do can compromise considerable accuracy; FastSPICE doesn't have big requirements in designer setup time and has better accuracy (albeit at longer simulation times). Generality, accuracy and runtime of FastSPICE simulators has improved greatly in recent years, to the point where they are now used to simulate full chips at the transistor level; as a result FastSPICE simulators have an enviable adoption record. Behavioral modeling and FastSPICE aren't necessarily mutually exclusive either: designers can choose to use a mix, essentially turning the dial on speed vs. accuracy.

The Near Future: Designers will increasingly employ behavioral modeling for testbench development. Transistor-level FastSPICE simulation will remain popular, while behavioral modeling will gain usage where simulation speed is more critical than simulation accuracy.

1.3 Front-End Performance Optimization

Current Status: Performance optimization at the transistor level is becoming increasingly popular for designing high performance analog designs, for migrating analog and custom digital designs to new process technology nodes, and for creating high-speed, low-power digital cell libraries. Since performance optimization requires up-front setup of constraints, its adoption for lower-performance analog circuits is more limited. Thus, if designers can easily meet the design specs using manual design techniques, they are less likely go through the setup effort to use an optimizer.
The Near Future: Adoption of optimizers will continue for high-performance analog design, for design migration, and for digital library creation. For optimizers to be valuable in the other areas of analog design, the optimizer must be an integral part of the design environment. The setup effort to use the optimizer must be a minimal increment on top of the existing manual design process. With FastSPICE / behavioral modeling and the appropriate hierarchical design methodology, performance optimization will find its way into use at the system level as well.

1.4 Yield Analysis and Optimization

Current Status: Performing process variation analysis, such as Monte-Carlo simulation, continues to be popular in the IDMs (Independent Device Manufacturers) where the designer has easy access to statistical process data. IDMs successfully improve their chip yields using variation analysis. Variation analysis is less popular in fabless design houses because accurate statistical process data is currently harder to come by, so process corners are typically used there. Modern variation analysis techniques not only inform the designer about how their design is going to yield but also point them to the problem devices in the circuit that are causing the yield problems.

The Near Future: Semiconductor devices sizes are shrinking, causing process variation effects to have a much larger impact on a circuit's performance and yield. Designers will increasingly use variation analysis to maintain reasonable yields on analog and high-performance digital circuits built on 90, 65 and 45 nm processes. Foundries are providing better and better statistical information, just in time for the fabless houses. To further improve yield, designers will be analyzing not only process variation effects but also layout variation effects, such as interconnect and special variation effects.

1.5 Layout Awareness, Layout Automation

Current Status: Layout-versus-schematic tools, parasitic extraction tools, and parasitic back-annotation into schematics are standard; even schematic-driven layout tools are common. For layout design itself, parameterized cells (Pcells, i.e. automated layout building blocks), are near-standard. Once a company has the Pcell infrastructure in place, layout design rules are taken into account during the design phase with little or no extra effort on the designer's part. Tools that fully automate standard cell layout are also popular among digital standard cell library designers. These tools can automatically create predictable layouts for hundreds of digital standard cells that require little to no modification by the layout engineer. As for layout automation in analog design, partial automation such as point-to-point routing is widely used. For fully automated placement and fully automated routing, adoption is mixed; the best traction to date has been in process migration and ECO. The up-front efforts needed to configure constraints are a critical issue, though CAD work continues to reduce this problem.
The Near Future: As chip speeds increase, the tightness of information coupling between front- and back-end design will increase accordingly. We'll move from "layout-aware front-end design" and "electrically-aware layout" to broad use of a unified database at the front- and back-end that all tools use.

1.6 Analog Structural Synthesis

Current Status: Transistor-level structural synthesis, the automatic generation of a circuit topology from supplied constraints, has been a long-time dream. But there are challenges. The synthesized circuit must work across all process and environmental conditions, and must be easy to lay out. The synthesis setup effort must be much easier than designing the circuit by hand. Finally, the overwhelming challenge is that the synthesized result must ultimately be silicon-accurate, and *trustworthy*. While a few academic synthesis prototypes have shown promise on well-constrained problems, to date no scalable analog structural synthesis technique achieves these goals.
The Near (Far?) Future: For structural synthesis to be adopted, one needs to invent a synthesis solution that meets the above criterion.

1.7 Conclusion

Has analog circuit design changed in the past 30 years? Indeed it has! In addition to the algorithmic advancements discussed above, schematic and layout capture tools have certainly proven to be a large improvement over manipulating circuits in text-based formats. The shift in label from "analog" to AMS signifies a trend towards system-level design. Going forward, time to market pressures will encourage designers to try out, and adopt, new automation methodologies. To gain industry adoption, a new analog CAD tool must require minimum setup. Minimizing the setup effort means new automation tools must be easily extendable from the existing design methodologies. Similar to how new simulation techniques reuse the same netlist and device models, new environments for setting up analog automation must naturally extend from the manual design setups. Open database frameworks such as OpenAccess should help reduce the setup effort by facilitating data compatibility and reuse between tools. Lastly, for designers to adopt a new automation tool, the new tool must help them solve real design problems that are difficult to tackle with the existing design methodology.