Enhanced Error Vector Magnitude (EVM) Measurements for Testing WLAN Transceivers*

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ABSTRACT

As wireless LAN devices become more prevalent in the consumer electronics market, there is an ever increasing pressure to reduce their overall cost. The test cost of such devices is an appreciable percentage of the overall cost, which typically results from the high number of specifications, the high number of distinct test set-ups and equipment pieces that need to be used, and the high cost of each test set-up. In this paper, we investigate the versatility of EVM measurements to test the variable-envelope WLAN (Wireless Local Area Networks) receiver and transmitter characteristics. The goal is to optimize EVM test parameters (input data and test limits) and to reduce the number of specification measurements that require high test times and/or expensive test equipment. Our analysis shows that enhanced EVM measurements(optimized data sequence and limits, use of RMS, scale, and phase error vector values) in conjunction with a set of simple path measurements (input-output impedances) can provide the desired fault coverage while eliminating lengthy spectrum mask and noise figure tests

1. INTRODUCTION

RF test is becoming a production bottleneck as the complexity of the RF devices increase to satisfy demanding performance requirements. The most important factor that contributes to the RF test cost is the long test times and complex test equipment that are required to perform various performance characterizations. For instance, there are over one hundred performance tests for RF transceivers, many of which are quite complex and require long test times [13].

To reduce the cost of testing RF devices, it is desired to compact the long test list into a smaller list which provides the same coverage. Fortunately, the performance parameters of a module are interrelated, obviating the need to test the complete set of performance parameters. However, the determination and optimization of the tests that require measuring a subset of specification parameters while ensuring the product quality may be challenging. The optimum test set for a system generation may not be the optimum for another due to the distinct characteristics of these systems. Therefore, product-specific architectural and behavioral characteristics should be utilized to determine the optimum test set.

As the design complexity increases and the time to market windows shrink, accurate simulations of the designs contribute a valuable insight to the manufacturing process. Lin *et. al.* discuss the correlation of actual EVM measurements to the computer simulations that utilize a specification level modeling of a power amplifier [12], and report that EVM can be predicted accurately through simulations. In order to reduce the test time, product specific characteristics prove to be useful in the optimization of certain test types. Helfenstein *et. al.* present an EVM calculation method under production conditions for GMSK modulators [9].

In order to reduce the test equipment costs, more simplified test solutions are suggested. Single tone [15] and two tone [10] signals can be provided for testing products that require modulated signal input. Unfortunately, these methods are inadequate for spread spectrum systems that utilize many subcarriers to increase the bandwidth efficiency. Recently, EVM-testing has received a lot of attention from the industry as a low-cost solution [8][9][5]. However, before resorting to EVM testing, and shipping products out relying on EVM, its usefulness should be extensively evaluated.

In this paper, we concentrate on WLAN transceivers implementing the IEEE 802.11a standard [1]. We investigate the versatility of EVM measurements on the transmit and the receive paths and analyze the capability of EVM testing in terms of distinguishing the defective circuits from the acceptable ones. Since EVM is very sensitive to many impairments in the transceiver, particularly for a variable envelope modulation scheme, it can be utilized as a low-cost alternative to other lengthy standard-compliance tests. We first show that EVM testing alone cannot provide the desired fault coverage. However, if optimized, EVM testing can reduce the test time and test setup cost for RF circuits by eliminating many of the lengthy and costly test setups such as noise figure and spectrum mask measurements. We present an input stimulus and test limit optimization method for EVM testing and a multi-layered fault injection, test evaluation, and test selection approach based on the detection capability, set-up cost, and the test time of each

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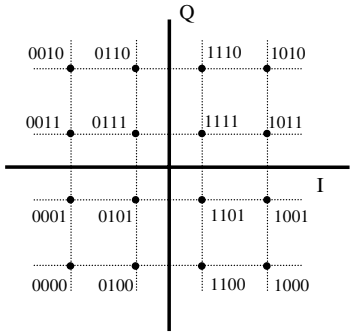


Figure 1: IQ Constellation

test. We show that testing a combination of EVM and a set of system level specifications (input-output impedances) can ensure the product quality.

2. OVERVIEW OF WLAN

WLAN systems are becoming more prevalent in the market as the use of wireless computers increases. WLAN systems implement the IEEE 802.11a standard, utilizing OFDM for channel modulation and phase shift keying (PSK) and quadrature amplitude modulation (QAM) schemes. PSK schemes are generally utilized at lower data rates to guarantee communication under low reception qualities. When the reception quality is high, QAM schemes with higher data rates can be utilized. This variable envelope scheme is spectrally very efficient. However, it imposes stringent requirements on the linearity of the receiver as well as the transmitter.

2.1 Digital Modulation and OFDM

A majority of digital modulation schemes employ In-phase and Quadrature components to utilize the bandwidth efficiently. I and Q vectors span a plane in which each transmitted symbol can be represented in a constellation diagram. Figure 1 illustrates a 4-bit quadrature amplitude modulation (QAM) constellation diagram. Each constellation point is assigned a symbol value.

In the IEEE 802.11a standard, transmitted data is divided into frames; each frame contains a header sequence and the data. The main purpose of the header sequence is to characterize the transmission channel, which may rapidly change due to certain environmental conditions. The header consists of a preamble of 12 symbols: 10 short symbols for signal detection, AGC (Automatic Gain Control), diversity selection, coarse frequency estimation, offset estimation and timing synchronization; 2 long signals for fine tuning of the channel frequency and offset estimation; and the SIGNAL sequence which identifies the rate and length of the following data.

2.2 WLAN Standard Tests and Test Cost

There are various specifications determined by the standard to ensure inter-operability. In order to verify the compatibility of the product with the standard, various test setups might be required. Unfortunately, verification of all specifications through dedicated measurement set ups can be costly for high volume production. Compliance to the standards can be guaranteed by a compact test list that characterizes the failure scenarios.

Some of the specifications determined by the standard apply both to the receive and transmit chains. For instance, the port impedances must be 50 Ohms to ensure signal integrity.

Receiver Test

For the IEEE 802.11a receivers, various blocking scenarios are defined and the receiver is expected to yield a minimum specified SNR (Signal to Noise Ratio) in each case. These scenarios are typically too complex to generate in a production test environment. Alternatively, the RF system designers translate these standard-compliance specifications into system-level specifications, which are easier to test. The receiver specifications are typically given in terms of gain, noise figure, third order input intercept (IIP_3), filter characteristics, local oscillator (LO) spurs, LO isolation, and the second-order input intercept (IIP_2 -if the half-IF frequency is not sufficiently suppressed by the band or image filter).

The receiver specifications can be grouped in terms of test equipment complexity into three categories: gain, filter characteristics, LO isolation, and input impedance can be tested with single tone sinusoidal RF signals. IIP_3, IIP_2, and LO spurs require multi-tone input signals (typically two-tone) and spectral analysis. Finally, noise figure requires two accurate noise sources and sensitive equipment to analyze the noise power within the given bandwidth.

The test modules utilized in the standard receiver tests typically come with a single RF module in a production tester. However, recently, low-cost RF tester platforms are under investigation [16] and there is an incentive to limit the complexity of the test requirements to keep the tester cost down. As an example, if tests that require a two-tone RF signal are eliminated, the corresponding tester may have a lower cost. The test time associated with each of these tests follow the same pattern, with single-point measurements, such as path gain, being the fastest and measurements requiring fine spectral resolution requiring more time.

Transmitter Test

The problem with characterizing the transmitter is that its standard-compliance specifications are given over random modulated signals, which are harder to formulate into known system-level specifications. As a result, typically, a number of standard-compliance specifications, as well as a number of system-level specifications are given for the transmitter. The system level specifications for the transmitter include gain, IIP_3, IIP_2, and LO spurs. Standard-compliance specifications typically include spectral mask and modulation accuracy. For example, for the IEEE 802.11a standard, modulation accuracy is specified in terms of EVM, and for CDMA (Code Division Multiple Access), modulation accuracy is specified in terms of waveform quality factor [6].

The test cost of system level specifications (gain, IIP_3, etc) is similar to that of the receiver specifications. EVM measurements require a modulated RF signal for the receiver and a golden receiver platform for the transmitter. This setup will be discussed in more detail in the next section. Spectral mask test requires a fine resolution spectral analysis. For instance, the IEEE 802.11a standard suggests that the spectral mask be measured with 100 kHz resolution bandwidth and 30 kHz video bandwidth. These requirements might translate into expensive hardware and extremely long test times since the circuit operation is at high frequencies (5 GHz for the IEEE 802.11a standard).

Conceivably, testing all specifications determined by the standard independently is redundant. An optimum test list

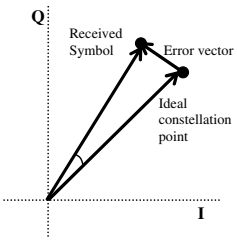


Figure 2: Error Vector Definition

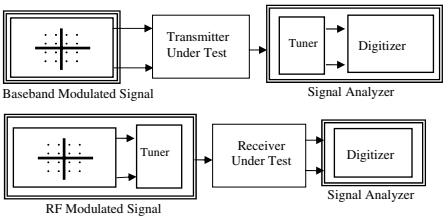


Figure 3: EVM measurement setup

derived from the characteristics of the product may provide shorter and cost efficient test solutions. Unfortunately, engineering of these specialized tests may require extensive development times and may be non-recurring [4]. Determination of tests that characterize a breadth of specifications and can be deployed to various generations of products is essential for test cost optimization.

3. OPTIMIZATION OF EVM FOR PRODUCTION TEST

The determination of the modulation accuracy is crucial for variable envelope systems where both the phase and the amplitude carry information. WLAN transceivers are designed to work with a number of distinct modulation schemes depending on the channel quality and the data rate. Under similar environmental conditions (the test environment), the most stringent specifications for the WLAN transceivers arise from the highest data rate case, i.e. the 4-bit symbol QAM case.

3.1 EVM

One of the most accepted modulation quality metric is EVM, which is the magnitude of the error vector between the received vector and ideal vector. A useful quantity derived from the error vector is the RMS value of the error vector magnitudes of all received symbols.

EVM is calculated by performing the complete recovery operation of the transmitted signal, including channel estimation, I-Q imbalance estimation and corrections. After the received signal is corrected and normalized, the RMS error between the expected (ideal) and received signal is calculated. The EVM calculation not only provides RMS value of the error vector magnitude but also the gain and quadrature error of the system, which can be utilized to characterize the overall path gain and phase shift of the system. The two additional parameters derived from the EVM calculation are *scale*, the scaling factor that normalizes the average power of the received signal, and the *phase*, the amount of rotation in the received signal constellation.

The allowable EVM values for each data rate are specified by the standard. Large error vector magnitudes are tolerable for low data rate systems, as long as the received symbols fall in their respective constellation region. However, as the system speed increases, these regions shrink and necessitate a more accurate demodulation for error free recovery of the transmitted signal. High bit rate systems, therefore, are required to produce lower EVM values to guarantee error free demodulation.

The IEEE standard imposes limits only on the RMS value of the error vector magnitude for the overall operation. However, both the phase and the magnitude of the error vector that are utilized for EVM calculation as well as the channel estimation provide additional pieces of information for test purposes. Moreover various system level parameters, such as path gain, can be determined during EVM calculation.

3.2 EVM Measurement setup

EVM measurements necessitate a modulated signal passing through the path. The modulated signal can be generated by the baseband processor of the product, if it is available and verified. In many cases, the digital baseband processor is usually tested separately and unavailable during the RF test, requiring an external baseband-modulated signal generator. These modules operate in the low-frequency domain. Modulating signals can also be generated using direct digital synthesis [13] within the tester. Thus, the cost of such baseband signal generators is typically not an issue. Figure 3 illustrates a standard setup where a transmitter and receiver can be tested. As the transmit upconverts the signal to RF frequencies, a tuner that downconverts the transmitted signal back to IF frequency is necessary. This tuner is fully characterized to calibrate the EVM measurements. Once the signal is acquired by the signal analyzer it can be digitized and the data can be transferred to the ATE (Automated Test Equipment).

The complementary operation should be performed to test the receive path. In this case, the modulated signal must be at RF frequencies, which might be generated by employing a tuner that upconverts the baseband modulated signal to required frequencies. The output of the receiver can be digitized and the data can be transferred to the ATE.

3.3 EVM Test Optimization

We consider two optimization schemes for EVM measurements: defining the data sequence to exploit the non-idealities in the circuit to the largest extend while reducing the test time and defining new test limits for EVM to increase its detection capability while avoiding yield loss.

Data Sequence Reduction

The preamble contained in the OFDM frame enables channel estimation in the field where the channel changes dynamically and noise and interferences co-exists. The complete preamble is not necessary in the controlled test environment allowing EVM to be measured through shorter sequences. The IEEE 802.11a standard suggests EVM measurement over randomly generated 20 frames with 16 OFDM symbols long. However, the EVM computation time for this sequence may demand unreasonable test resources since the EVM computation necessitates FFT operations requiring extensive data storage and computation capabilities. Furthermore, this random bit sequence might not produce corner cases such as large instantaneous EVM from switching one symbol to another. A shorter known sequence exploiting these corner cases may be more useful and reduce the test time appreciably.

We aim at reducing the number of symbols that need to be applied for EVM testing in our input sequence reduction approach. We first define a random data sequence of 320 symbols as defined by the standard. We go through this sequence and replace some of the symbols to ensure that the corner cases, such as large instantaneous switching from one symbol to the another, are included in this overall sequence. We then generate a small set of random circuit instances that mimic the variations in the manufacturing process. In addition, we generate another set of circuit instances with higher process deviations to mimic failure scenarios. These two sets of circuit instances constitute our input sequence *calibration set*. We then group the circuit instances in the calibration set as faulty or fault free based on their specifications (gain, IIP_3, NF, etc). We use this calibration set to evaluate the potential detection capability of EVM measurements (RMS, scale, and phase) for all the symbols. We set the EVM limits based on the response of the fault free circuits. Then we iteratively eliminate symbols which do not alter the overall detection capability of the measurements.

EVM Test Limit Determination

The EVM limits given in the standard are typically relaxed to test the operational health of the RF paths only. Some circuits that satisfy EVM specifications that is given in the standard might fail other specifications such as input-output impedances, spurious free dynamic range, and even the path gain. Since EVM has a potential for being a characterization quantity, which may allow significant reduction in the test time, tolerable product specific EVM values should be derived from the circuit architecture. While these EVM limits may increase the fault coverage, the ratio of rejected acceptable parts (yield loss) may also increase. The test setups that increase the yield loss are generally not desirable as a circuit labelled faulty by the test setup will likely to be discarded. However, if the fault coverage of a test set up is not adequate, the faulty circuits passing through the test setup are likely to be detected by other test setups. Therefore, the yield loss should be maintained at reasonable values, since it directly translates into revenue loss. In this work, we set the tolerable yield loss value to 1%.

In order to determine reasonable EVM limits that provide the maximum fault coverage with the minimum yield loss, we utilize two different sets of random circuit instances, which we call *training* and *verification* test sets. In order to ensure the robustness of the test method, both sets contain a statistically significant number of circuit instances and are generated by sampling from small and large process variation cases. Both sets contain a number of acceptable circuit instances as well as a number of faulty circuit instances, as determined by the specifications (Gain, NF, IIP_3, Spectral Mask, Z_{in}, and Z_{out}). The training set is utilized for test development. The maximum EVM of the acceptable circuits in the training set is utilized as the acceptable EVM limit. Any circuit instance that has a larger EVM than this limit is classified as faulty. This limit may be tweaked to attain the desired yield coverage. However, the desired fault coverage by using only the EVM test may not be adequate. In this case, additional test setups that provide the desired fault coverage can be included in the final test list.

The purpose of the verification set is to validate the test methodology. The verification set also should contain statistically significant number of circuit instances. The test setups and their limits determined from the training set must be utilized to calculate the fault coverage and the yield loss. Ideally, the fault coverage and the yield loss attained in the verification set should match the results found in the training set. If the fault coverage and yield loss values of the two distinct sets are not in agreement, the number of circuit instances in both sets need to be increased. The optimum size of these two sets can be determined iteratively by adding more samples, until the fault coverage and yield loss values agree.

4. DETECTION CAPABILITY OF EVM MEASUREMENTS

In order to replace various other costly tests and still ensure product quality, EVM testing should be able to locate real world failure scenarios in which multiple failures may occur at the same time. There are various test methods that target and detect catastrophic failures with simple procedures [2]. Unfortunately, most of the failures are marginal and cannot be characterized by simple tests.

Accurate fault modeling is essential for the evaluation of the success of EVM measurements. Modeling every failure scenario at the process level may not be possible. Therefore, fault models at the layout level (transistor widths/lengths, inductances, capacitances) and specification level (gain, input-output impedances) should be considered. Each performance parameter (IIP3, gain, noise figure, BER, EVM) have a certain quality assurance and associated test cost. In order to determine the optimum test set, the relations between the failure scenarios and the performance metrics should be studied.

4.1 Fault injection and Simulation

Unlike digital circuits where physical defects, such as opens and shorts, are the main cause of product failures, RF circuits are much more susceptible to process deviations. The much less dense RF circuits have a smaller probability of structural defects (opens and shorts) and when such defects are present, they can typically be detected through simple DC or low frequency tests [14][7]. Thus, for test development we concentrate on the much more challenging task of detecting circuit failures where the circuit functions but fails to meet the specifications. Such failures are caused by process deviations and the fault injection scheme should incorporate such process deviations.

In order to include a wide range of possible failure scenarios, various levels of the design hierarchy need to be considered. At the process/layout level, failures may be caused by local deviations, point defects, and general process variability. In these scenarios, multiple block-level or system-level parameters may be affected concurrently.

In addition, due to an unmodeled physical phenomenon, some block-level parameters may deviate independently. For example, the LO may generate spurs that cannot be modeled through process/layout level deviations due to the lack of accurate modeling of the PLL phase noise behavior at this level. As a result, it is essential that failure scenarios at process/layout level as well as block-level be considered.

In our fault injection scheme, all process, layout, and block level parameters are randomly selected from a distribution space, as shown in Figure 4. In order to cover a wide range of failure scenarios, we expand the distribution space of all parameters (the 6σ tolerance windows) beyond their tolerable variation margins given by the process. In other words, in

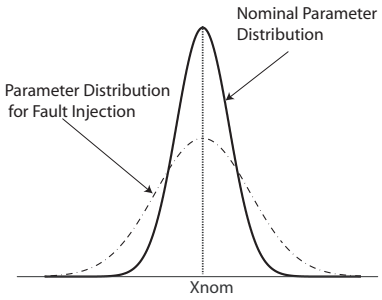


Figure 4: The distribution of circuit level and block level parameters used in Monte Carlo simulations

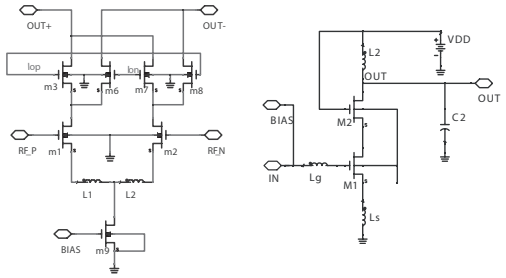
order to inject faults, we generate a wider distribution space for all parameters and randomly sample from this space. The circuit parameters may fall anywhere within the distribution window. Thus we avoid limiting the fault injection process to single point deviations. Even though the circuit parameters have larger variations in this wider distribution space, we only classify a circuit faulty if it violates any of the specifications.

4.2 Pass/Fail Criteria

Analog fault definition has always been a controversial issue. In the analog domain, typically a certain level of hierarchy has been chosen both for fault definition and pass/fail criteria determination [3]. For example, if the faults are defined at the circuit level (R, L, C), circuits with out-of-tolerance R, L, C values have been considered faulty. However, this definition is at odds with the design goals of making the circuit as robust to component deviations as possible. In this way, the above fault definition may result in large yield losses, and also test escapes since circuits with in-tolerance component values may still fail the specifications. A possibility to solve the yield loss issue is raising the level of fault definition. However, raising the level of hierarchy for fault definition (e.g. defining faults in gain, bandwidth, etc) results in overlooking correlations in these parameters, thus overlooking important failure scenarios.

In order to break this stalemate, we proposed to decouple fault injection from the pass/fail decision [3]. We use the same approach to EVM evaluation. According to the definition in [3], process variability, local deviations, and block-level deviations are injected into the circuit to generate possibly failing circuits. However, some circuits with injected deviations may not violate any of the system level specifications. Despite the fault injection, we label these circuits as *PASS*. If a generated circuit instance fails one specification, even with nominal process variability, then we label this circuit as *FAIL*. In this work, we use specifications that are defined in the standard as test limits. We determine the test limits for the remaining performance parameters, whose acceptable limits are undefined in the standard, by Monte Carlo simulations. In this paper, we use a 3% variation (3σ point) to mimic the nominal process, and a 15% variation (3σ point) to generate faulty circuit instances.

It is important to distinguish the pass/fail limits from the test limits. In some cases, one may impose tighter test limits than the specifications. If some parts fail the tighter test limits but do not fail any of the specifications, there will be a yield loss. While we use tighter test limits on EVM than mandated by the IEEE 802.11a standard, we



(a) Double balanced mixer (b) Cascode LNA

Figure 5: Transistor level mixer and LNA circuit

label circuits as faulty only if they fail another specification or the more relaxed standard-compliance EVM specification. Thus, our test limits for EVM and our specifications for EVM are different. In the next Section, we will discuss the effect of this tighter limit on yield loss.

4.3 Selection of System Level Tests

Based on fault injection and pass/fail decisions, faulty circuits may be detectable through multiple tests. Some faulty circuits may be detectable by only one type of set-up, making the corresponding test set-up essential. Such essential tests and the corresponding set-ups need to be included in the final test set.

The remaining failure scenarios may be detected by more than one test, each of which is associated with a set-up cost and a time cost. The set-up cost is collective; once a test set-up is included in the final set, subsequent tests using the same set-up incur no additional set-up cost. The test time cost is incremental; each test adds its time to the overall test time. Based on these observations, our goal during test selection is to detect all failing components while minimizing the set-up cost and the test time. Each of the optimization goals can be given a particular weight. We use a widely used simple heuristic based on immediate test coverage benefit and test set-up cost of each test [2], to select the final tests.

5. EVM FOR WLAN

The WLAN transceiver consists of a receiver and a transmitter operating at 5.3 GHz frequency band. We utilize the IEEE 802.11a standard modulated source generator of the Agilent Advanced Design System (ADS). The transmitter is modeled using a transistor level double balanced mixer and a power amplifier with adjustable gain, noise figure, IIP_2 and IIP_3 parameters. The synthesizer is modeled as a single monolithic oscillator by the addition of in-band phase noise (-80dBc/Hz nominal).

The receive path consists of a transistor level LNA circuit and the double balanced mixer for downconversion that is utilized in the transmit path. The LNA is a stability optimized version of the cascode LNA architecture [11][3]. The process node is $80nm$ and BSIM4 models are utilized for simulation. All circuits are designed and simulated at the transistor level using ADS. The LNA and mixer circuits are given in Figure 5.

5.1 Input Stimulus Optimization

In order to minimize the test time, the number of OFDM symbols that are utilized to measure the EVM should be minimized. Instead of using a pseudo-random sequence, an optimized sequence that exercises the non-idealities of the

CUT may provide a better understanding of the operational health of the circuit. We generate a calibration set which consists of 100 circuits with 3% process variability and 100 additional circuits with 15% process variability. The EVM parameters (RMS value, scale, and phase) are measured with the complete 320 OFDM symbols as suggested in the IEEE standard. The OFDM symbols that do not change the fault coverage or the yield loss are labeled redundant, and discarded from the stimulus one-by-one. During the calibration sequence, we are able to reduce the number of required OFDM symbols to 20. This method requires $80\mu s$ sampling time and 20 FFT operations, as opposed to $1.3ms$ sampling time and 320 FFT operations as given in the standard.

5.2 Receiver Test Optimization Results

The training set for the receiver consists of 2000 instances of the circuit with 3% variability in process, layout, and block parameters and 2000 instances of the circuit with a 15% variability. Out of 4000 random circuit instances, we have 2098 passing circuits and 1902 failing circuits based on the specifications which include gain, noise figure, IIP_3, input impedance, and output impedance. The training set and the verification set are non-overlapping and faulty and fault free circuit instances are randomly distributed over these two sets. The main purpose of the training set is to determine the EVM limits and the additional test setups that may be needed to increase the fault coverage. The EVM limits for RMS value, phase shift, and the scaling factor are found to be 1.5%, 0.4 Radian, and 8.1 dB, respectively.

Any circuit instance that has larger EVM than these limits is labelled as faulty. Narrower EVM limits than this value may cause the rejection of acceptable parts, thus yield loss. This value should be maintained at reasonable values in order to increase the revenue. Table 1 depicts the fault coverage and yield loss of the EVM test. The fault coverage and yield loss values obtained from the verification set are very close to that of the training set, indicating the robustness of the test limits determined during test development. Observe also that the fault coverage is limited when the test set solely consists of EVM measurements. In order to increase the fault coverage, additional test setups need to be added to the test set. For this architecture, the tests that are needed to maintain adequate fault coverage are Z_{in} and Z_{out}, which increases the fault coverage to 98%. The remaining traditional test setups (IIP_3, $Gain$, and NF) are eliminated. Based on the results, and the test selection technique, the final test set includes {EVM, Z_{in}, and Z_{out}}. Noise figure and IIP_3 tests are costly and lengthy tests, the elimination of which can reduce the test cost appreciably.

5.3 Transmitter Test Results

Similarly, the transmitter training and verification circuit instances are generated with 2000 samples each. Out of the 4000 circuit instances, 2048 circuits are labeled as fault-free and 1952 instances are labeled as faulty based on gain, IIP_3, input impedance, output impedance, and spectrum mask specifications. The EVM limits for RMS value, phase shift, and the scaling factor are found to be 2.4%, 1.8 Radian, and 4.7 dB, respectively. Table 2 summarizes the fault coverage and the yield loss of EVM measurements for the transmitter. Note that the EVM measurements eliminate Spectral Mask and IIP_3 measurements, which generally demand extreme test resources.

Based on the test selection methodology, the set {EVM, Z_{out}, Z_{in}} provides 98% fault coverage with a 1.4% yield loss. Note that once again the yield loss and the fault coverage values for the training set and the verification set are in agreement, indicating that 4000 samples are adequate for test development.

5.4 Illustrative Measurement Results

While we do not have the capability to conduct measurements on large and diverse set of good and bad chips, in this section we present sample measurement results of chips that violate several specifications on the transmitter and the receiver and compare these with the results of EVM measurements. The goal of these experiments has been to show examples of our simulation-based findings. For bench measurements, we use commercially available RF products. Thus, the circuits used in the measurements are different from the ones used in test development. These measurements are only to illustrate one of our findings, namely that EVM testing can replace spectrum mask testing. The measurements are conducted using bench equipment. The IEEE 802.11a standard waveform is created using ADS and vector signal generator (Agilent E4438C), output waveforms are captured through a Vector Spectrum Analyzer (VSA) (Agilent 89600S), and the parameters are calculated using MATLAB and VSA software.

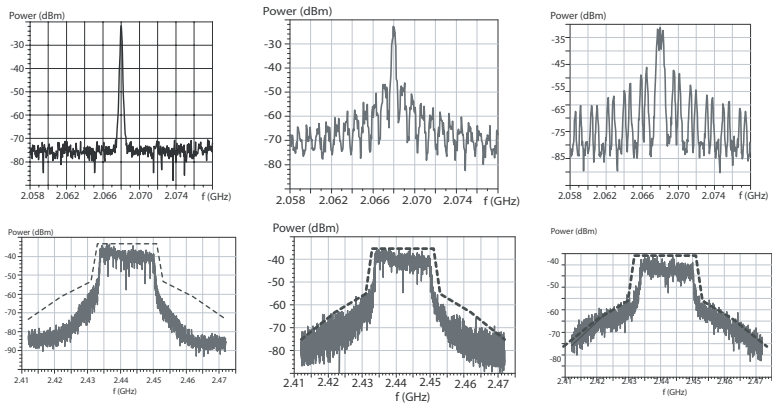
For the transmitter, the major conclusion of our work has been that EVM testing, which require 200ms test time, can replace the time consuming spectrum mask testing, which require 800ms on this bench setup. We have conducted measurements on two bad samples that violate the spectrum mask; the violations are as a result of the unacceptably high phase noise and spurs of the local oscillator. Figure 6 shows the spectrum of the local oscillator signal and the spectrum of the modulated RF signal for three chips. Figure 6(a) shows the local oscillator and RF spectrum for a good chip. Figure 6(b) shows the same measurements for an unacceptable chip with marginal spectrum mask violations. Finally, Figure 6(c) shows the measurements for an unacceptable chip with high spectrum mask violations. In both faulty cases, the EVM measurements can easily flag these chips as

	Training Set		Verification Set	
Measurement	**YL(%)**	**FC(%)**	**YL(%)**	**FC(%)**
EVM Only	1.3	75	1.3	75
EVM +Zin+Zout	1.3	98	1.3	98

Table 1: Yield Loss (YL) and Fault Coverage (FC) of the Receiver Tests

	Training Set		Verification Set	
Measurement	**YL(%)**	**FC(%)**	**YL(%)**	**FC(%)**
EVM Only	1.3	79	1.4	80
EVM +Zin+Zout	1.3	98	1.4	98

Table 2: Yield Loss (YL) and Fault Coverage (FC) of the Transmitter Tests



(a) acceptable case EVM = 0.02 (b) phase noise violation EVM = 0.8 (c) high phase noise violation EVM >0.95

Figure 6: Bench measurement results for a good chip and two faulty chips

faulty.

6. CONCLUSION

In this paper, we present a detailed test analysis of WLAN transceivers, with particular emphasis on exploring the use of EVM testing for the receiver and the transmitter. The variable envelope modulation scheme of the IEEE 802.11a standard makes EVM very sensitive to non-idealities in the transceivers, which can be used to provide efficient testing.

We first reduce the symbol length of EVM measurements in order to reduce the test time. We then optimize the EVM measurements by defining narrower limits than mandated by the standard to enhance its detection capabilities. However, the narrower limits are carefully chosen not to result in unacceptable yield loss. We generate a circuit model for the WLAN transceivers using transistor level circuits as well as block level failure injection schemes. We decouple the fault injection from the pass/fail determination to ensure that yield loss is minimal and present a test selection technique that aims at minimizing the test set-ups cost as well as the test time.

Based on our analysis, optimized EVM can reduce the test time and test cost for WLAN transceivers, while keeping the yield loss to around 1%. When complemented with a number of easily measurable system specifications, such as input-output impedances, EVM testing provides nearly perfect coverage for all the failure scenarios. The most important conclusion from our analysis on the transmitter is that EVM can detect all the failure scenarios that lead to the violation of the spectral mask requirements, enabling the elimination of this costly and lengthy test. Our analysis of the WLAN receivers indicates that EVM testing can replace IIP_3 and NF measurements, enabling test cost and test time reduction. While our test development results are circuit dependent, the methodology that we present in this paper can be applied to any RF WLAN circuit to generate high quality, robust, and lower cost test sets.

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