A Novel Framework for Faster-than-at-Speed Delay Test Considering IR-drop Effects

Nisar Ahmed, Mohammad Tehranipoor
Dept. of Electrical & Computer Engineering
University of Connecticut
tehrani@engr.uconn.edu

Vinay Jayaram
Texas Instruments, Inc.
Dallas, TX
vjayaram@ti.com

Abstract

Faster-than-at-speed test have been proposed to detect small delay defects. While these techniques increase the test frequency to reduce the positive slack of the path, they exacerbate the already well known issue of IR-drop during test. This may result in false identification of good chips to be faulty due to IR-drop rather than small delay defects. We present a case study of IR-drop effects due to faster-than-at-speed test. We propose a novel framework for pattern generation/application using any commercial no-timing ATPG tool, to screen small delay defects and a technique to determine the optimal test frequency considering both performance degradation due to IR-drop effects and positive slack.

1. INTRODUCTION

Transition fault model is widely practiced in industry to test delay-induced defects and it is a cost-effective alternative to functional pattern generation [1][2]. Traditionally, transition fault tests were generated assuming a fixed cycle time for each clock domain (generally delay tests are generated/applied one clock domain at a time). Under the above assumption, a delay defect will be detected only when it causes a transition to reach an observe point (primary output or scan flip-flop) by more than the positive slack of the affected path. Slack of a path is a measure of how close a transition on the respective path meets the timing to an observable point, relative to the test cycle time.

A delay defect with defect size not large enough to cause a timing failure under the fixed cycle time notion is referred to as a small delay defect. A small delay defect might escape during test if is tested using a short path. While the same defect might be activated on a longer path during functional operation and it may cause a timing failure. Also, small delay defects might become a *reliability* issue as the defect might magnify during subsequent aging in the field and cause a failure of the device. Hence, it is important to detect such defects during manufacturing test using efficient techniques [3].

There is a growing industry concern for timing aware ATPG tools. Although most of the widely used commercial ATPG tools are still timing unaware and generate test patterns based on the ease of finding an affected path, instead of a least slack path. Encounter True-Time Delay Test Tool ™[4] uses actual design timing (Standard delay format (SDF)) information for ATPG. While it still uses efficient ATPG algorithms and pseudorandom data to achieve high coverage in fewer patterns, it uses back-annotated timing information (SDF) to apply them at faster-than-at-speed. It sets the transition test capture frequency based on the slack of the paths exercised and also includes the ability to test non-critical paths faster-than-at-speed for small delay defects. The possible limitations of such techniques are: 1) the SDF must be calibrated with very high accuracy to correspond with the tester operating conditions and 2) the timing information must also take into account the process variation effects and dynamic effects, such as the IR-drop and crosstalk.

1.1 Related Prior Work

Various techniques have been proposed in the past for improving the small delay defect screening quality of a pattern set. A number of these methods such as very-low-voltage (VLV) [5] and burn-in [6], modify the operating conditions of test environment and magnify the defect size, which escape at nominal conditions. However, in DSM designs, the effectiveness of VLV testing is reducing as I) the scaling of threshold voltage is not proportionate to supply voltage and II) issues like IR-drop and crosstalk are becoming more prominent and burn-in is associated with considerable high costs.

In [7], a new transition fault model, called As Late As Possible Transition Fault (ALAPTF) was proposed. The method tries to activate and propagate a transition fault at the target gate terminal through the least slack path possible. The ATPG method used is complex and will be more CPU intensive compared to a no-timing ATPG. In [8], the authors proposed a new ATPG tool to generate K longest paths per gate for transition fault test. The technique targets all the transition faults to find the longest path(s). A longest path does not reflect the detectable delay defect size. For example, if the least slack path of a gate is a short path then a small delay defect on such a gate output cannot be detected for the nominal frequency.

The technique proposed in [3] is based on detecting a smaller delay on a shorter path by increasing the frequency of operation. The method groups a conventional delay fault pattern set into multiple pattern sets which exercise almost equal-length paths. The different pattern sets are then applied at different frequencies to detect smaller delays. Due to increasing the frequency, the capture edge might occur in the hazard region for some of the observation points. To enhance the effectiveness of screening frequency dependent defects, the authors in [9] proposed a pattern selection methodology to reduce the delay variation of the selected pattern set and higher frequency is used for pattern application. The method uses a multiple-detect transition fault pattern set and it uses statistical timing analysis techniques to reduce pattern delay variations. The above methods may also be limited by the highest possible fre-

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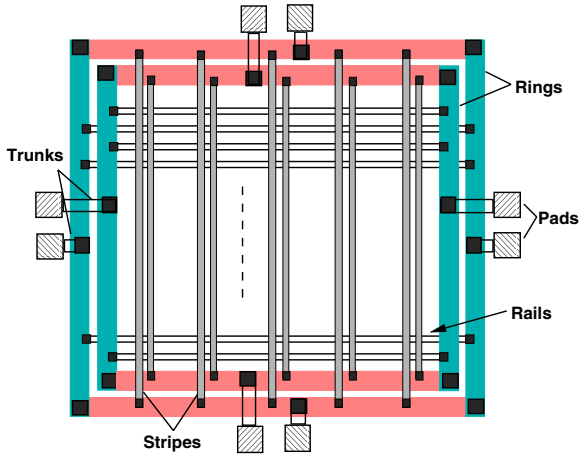

Figure 1: Power/Ground Distribution Network.

quency of operation which exacerbates the already well known issues of peak power during test and IR-drop.

1.2 Our Contribution

Most of the above proposed techniques for screening small delay defects take advantage of applying the patterns at higher frequencies to reduce the positive slack of the paths. Increasing the frequency impacts the performance of the chip due to adverse IR-drop effects. In this work, we present the practical issues during faster-than-at-speed delay tests. We present a case-study of a design and illustrate the increase in both peak and average IR-drop effects due to faster-than-at-speed pattern application. Increase in IR-drop directly relates to performance degradation due to effective voltage reduction reaching the gates in the circuit.

Also, we propose a novel framework for the application of transition fault patterns. The technique groups the transition fault test patterns generated using any commercial ATPG tool (here Synopsys Tetramax [10]) into different groups based on the maximum path delay affected in each pattern. We then perform an IR-drop analysis on each group based on the switching activity and determine the maximum frequency of pattern group. This reduces the risk of any false identification of good chips to be faulty due to IR-drop effects rather than small delay defects.

The rest of the paper is organized as follows. Section 2 explains a case study with detailed pattern delay and IR-drop analysis for faster-than-at-speed test pattern application. The framework with pattern grouping technique and determination of optimum test clock period is discussed in Section 3. The experimental results are presented in Section 4. Finally, concluding remarks are in Section 5.

2. CASE STUDY

In this section, firstly we describe the physical design implementation and a transition fault pattern delay analysis. We, then present a detailed IR-drop analysis and related performance degradation due to effective voltage reduction for a transition fault test pattern at rated functional speed and faster-than-at-speed application to detect small delay defects.

2.1 Physical Design Implementation

For our experimentation, we had selected an ITC'99 benchmark design $b19$ and the physical design implementation was performed using Cadence SOC Encounter place and route tool [11]. The

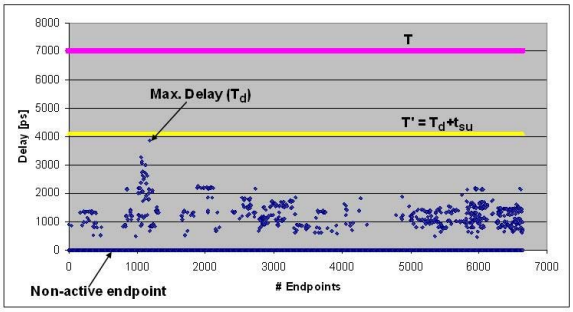

Figure 2: Path delay distribution to all endpoints for a single launch-off-capture transition fault test pattern ($b19$ benchmark).

design contains almost 219K gates, 51 IO pads, and about 6,642 flip-flops. Scan-based test insertion was performed using Synopsys DFT Compiler [10] with eight scan chains and a slow speed scan enable is used for launch-off-capture transition fault test. During physical design, the design is timing closed for an operating frequency of 142MHz at nominal operating voltage ($1.8V$) and temperature (25^oC) conditions. A slow scan shift speed of 10MHz was used. It is implemented in $180nm$ standard cell library [12].

The power-planning for the design was performed assuming a net toggle probability of 20% during functional operation. Figure 1 shows the power/ground distribution network of the chip. Power rings ($width = 20\mu m$) were created using higher-level routing layers (Metal5 and Metal6) and carry power around the standard cell core area. Four power (VDD) and ground (VSS) pads each were inserted and connected to the respective rings with wires referred to as trunks. After creating the power rings, power and ground is routed to the standard cells using stripes and rails. The stripes ($width = 10\mu m$) were created using routing layer Metal4 and a distance of $100\mu m$ between adjacent stripes connecting power rings. The design was then placed and routed along with clock-tree synthesis and scan cell ordering to minimize scan chain wirelength. In order to determine a quick estimate of IR-drop, the design net parasitics (resistance and capacitance) were extracted using a 3-D extraction tool (Synopsys STAR-RCXT [10]). The average statistical IR-drop using vector-less approach was measured for both VDD and VSS nets considering 20% net toggle probability. The results showed 2.8% voltage drop in VDD and a voltage bounce of 4.5% for the VSS net, which can be considered negligible. It will illustrated in the following sections that the actual IR-drop during transition fault test patterns is much higher compared to statistical IR-drop due to high switching activity.

2.2 Pattern Delay Analysis

The ATPG algorithms are based on zero-delay gate models and the existing tools are timing un-aware for pattern generation process and generate test patterns based on the ease of finding an affected path, instead of a least slack path. Figure 2 shows the path delay distribution of a single transition fault test pattern across all endpoints, generated using a commercial ATPG tool (Synopsys Tetramax [10]). The pattern was simulated using the design timing information of the gates and the extracted parasitic interconnect delay information at nominal operating conditions (25^oC and $1.8V$). An observation point at the end of a path (primary output or scan flip-flop) is referred to as an *endpoint*. Since, the primary outputs are not observed due to insufficient timing accuracy of a low cost tester to strobe the primary outputs at functional speed [1][13], here, an *endpoint* refers only to a scan flip-flop.

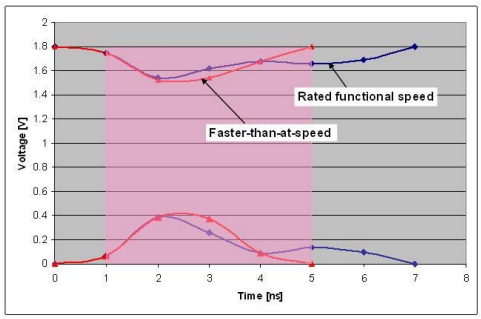

Figure 3: IR-drop effects for rated functional speed and faster-than-at-speed of a transition fault test application ($b19$ benchmark).

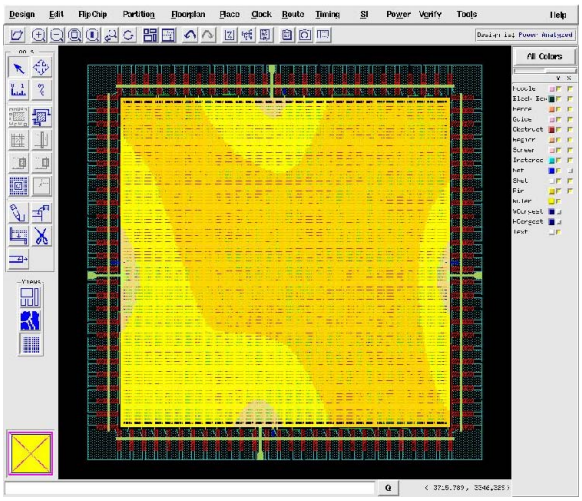

Figure 4: IR-drop plot in VDD net for the transition fault test pattern at rated functional frequency f ($b19$ benchmark).

The functional clock period ($f = 142MHz$) is represented by $T = 7000ps$. An endpoint which does not observe a transition, referred to as a *non-active* endpoint, is represented by zero delay. It can be noticed that only a subset of endpoints observe transitions. These are referred to as *active* endpoints. In this particular pattern, the maximum path delay to an active endpoint is $T_d = 3860ps$. In order to increase the small delay defect screening capability, based on the maximum path delay (T_d), the test clock timing can be adjusted to $T' = T_d + \tau_{su}$, where τ_{su} is the setup time of the scan flip-flop. This improves the small delay defect screening capability of the test pattern as the path delay affected by the pattern is relatively close to the clock period (near zero slack). For this particular pattern with the delay distribution shown in Figure 2, the faster-than-at-speed clock period was selected to be $T' = 4060ps$ ($f' \simeq 245MHz$), where $\tau_{su} = 200ps$. Note that, for the purpose of clarity in explanation, we did not consider the timing margin for process variation effects, which can be easily incorporated.

2.3 IR-drop Analysis

In this section, we analyze the IR-drop effects when a transition fault test pattern is applied at rated functional frequency (f) and the consequences of increasing the test frequency (f') for detecting small delay defects. We define the IR-drop at rated functional frequency and faster-than-at-speed frequency as *inherent IR-drop* and *faster-than-at-speed IR-drop*, respectively. To measure the IR-drop of the pattern, the switching activity inside the circuit was captured

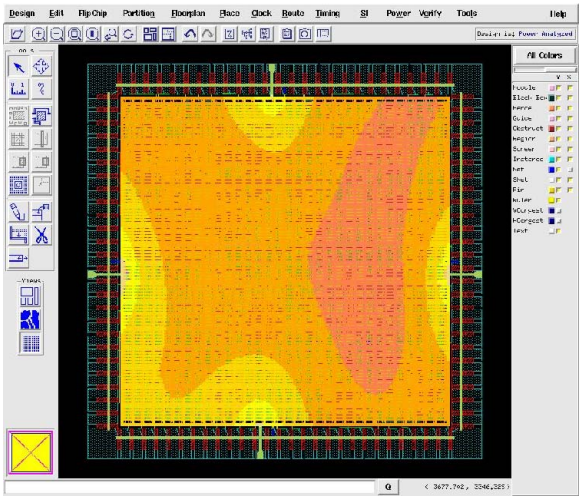

Figure 5: IR-drop plot in VDD net for the same transition fault test pattern at faster-than-at-speed frequency ($f' = 1.7 \times f$) ($b19$ benchmark).

in the standard value change dump (VCD) format during gate-level timing simulation. The switching activity information (VCD file) along with physical design and technology library information is used by SOC Encounter tool [11] to estimate the IR-drop of the pattern.

Figure 3 shows the VDD (VSS) voltage waveforms during the at-speed launch and capture cycles of the pattern. To measure the *inherent IR-drop* at rated clock frequency, the launch-to-capture window ($7ns$) was split into $1ns$ time frames and average IR-drop was measured in each time frame. Since the clock insertion delay (delay from chip clock pin to scan flip-flop's port) was approximately $1ns$, the voltage drop/bounce effect starts from $1ns$. It can be noticed that the effect of IR-drop is maximum in the beginning of the clock cycle due to high simultaneous switching activity and gradually decreases. Also, a secondary IR-drop peak can be observed around $5ns$ due to the negative clock edge switching activity in the clock network, since the clock waveform used was 50% duty cycle (equal time for logic 0 and 1).

As the test frequency is increased, the IR-drop increases due to two factors: 1) increased data path switching speed and 2) shifting of the negative clock edge switching activity in the clock network towards the early cycle period compared to the rated functional frequency. This results in increase of both peak and average IR-drop due to faster-than-at-speed patterns as shown in Figure 3. The peak IR-drop for VDD increased from $0.25V$ to $0.27V$ (approximately by 8%) and the average IR-drop measured across the time frame 1-$5ns$ (shaded region shown in Figure 3) considering both VDD and VSS ($V_{VDD,IR-drop} + |V_{VSS,IR-drop}|$) increased from $0.26V$ to $0.33V$ (approximately 15%). The IR-drop region is selected based on the delay distribution of the endpoints in the pattern, i.e. all the transitions in the pattern fall in this particular region.

Figures 4 and 5 show the IR-drop plots on the power (VDD) network for the transition fault test pattern at functional operating frequency ($f = 142MHz$) and at faster-than-at-speed test frequency ($f' = 245MHz$) which is approximately 1.7X greater. The IR-drop plots were obtained from the Cadence SOC Encounter tool [11] measured across 1-$5ns$ time frame (shown in Figure 3). Note that, with increased clock frequency, the IR-drop in most portions of the chip increases which results in reduced effective voltage difference between the VDD and VSS ports observed by each gate. This re-

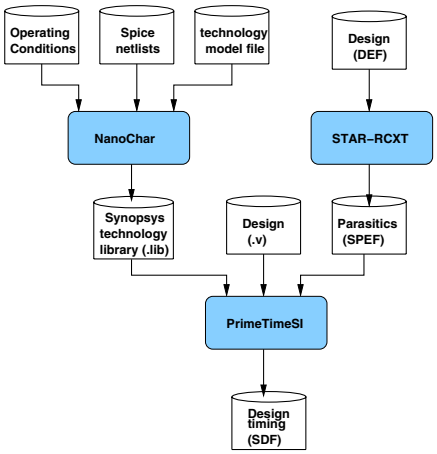

Figure 6: Timing Calculation at different operating voltage conditions using Synopsys design tools [10].

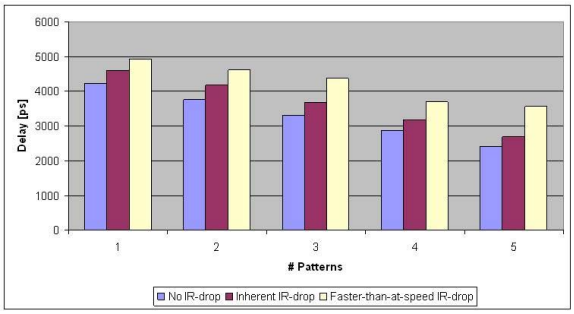

Figure 7: Maximum path delay of five transition fault test patterns in three cases applied to $b19$ benchmark: Case1) No IR-drop, 2) *inherent IR-drop* and 3) *faster-than-at-speed IR-drop*.

sults in performance degradation of the circuit. Therefore, it is very important to consider the performance degradation due to IR-drop effects along with the positive slack when frequency is increased for small delay fault detection.

2.4 Performance Degradation Due to IR-drop Effects

As shown in Figure 5, increasing the frequency has adverse impact on IR-drop across the chip. In this section, we show performance degradation of the chip due to effective voltage reduction related to *faster-than-at-speed IR-drop*. After determining the average IR-drop of a transition fault test pattern during the launch and capture window, to measure the performance degradation, we need to generate the design timing information at the new operating voltage condition considering the voltage reduction due to IR-drop. The standard cell technology library (.lib) file contains the timing information of each gate in the design at a particular operating condition (process, voltage and temperature). The parasitics (coupled resistance and capacitance values) extracted during physical design in standard parasitic exchange format (SPEF) can be used by any delay calculation tool to estimate the interconnect delays.

Figure 6 shows the flow of generating the design timing information including detailed parasitics at different operating conditions. The technology library is characterized using Synopsys NanoChar [10] library characterization tool for the new operating voltage ($V_{DD} - V_{IR-drop}$). We used Synopsys PrimeTimeSI [10] delay calculator to generate the timing information. It essentially reads the design, technology library and parasitics and generates the design timing in SDF format at the respective operating voltage. We generated two SDF files at voltage conditions considering *inherent IR-drop* and *faster-than-at-speed IR-drop*. These generated SDF files were back-annotated during gate-level verilog timing simulations to measure the performance degradation. Figure 7 shows the maximum path delay for five different patterns in three different cases: Case1) no IR-drop effects, Case2) *inherent IR-drop* at functional frequency and Case3) *faster-than-at-speed IR-drop*. The performance degradation due to *faster-than-at-speed IR-drop* increases by up to 20% and 9% compared to no IR-drop effect and *inherent IR-drop*, respectively. For the pattern considered earlier during this case study, the maximum pattern delay for faster-than-at-speed application increased from $3860ps$ to $4610ps$ which is well beyond the fast-than-at-speed clock period ($T' = 4060ps$) resulting in functional timing failure. This pattern failure occurred due to IR-drop effects rather than any small delay defect. Therefore, it is very important to consider the IR-drop effects during faster-than-at-speed application along with the positive slack for detecting small delay defects.

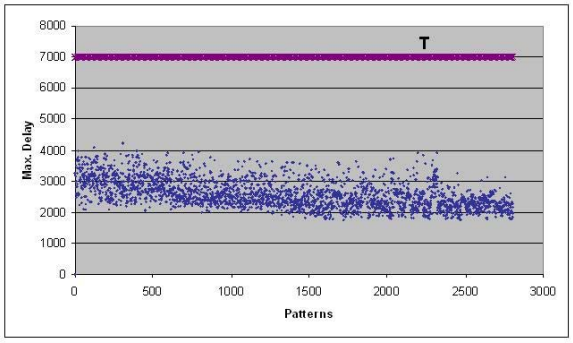

Figure 8: Maximum path delay affected in each pattern of transition fault pattern set (*b19* benchmark).

3. FRAMEWORK

As explained in Section 2, to improve the small delay defect screening capability of a test pattern, the timing can be adjusted such that the path delay affected by a pattern is relatively close to the clock period (*pattern slack* near zero). However, the performance degradation due to IR-drop effect also needs to be considered to avoid any good chips failing the test. Since, the transition fault pattern set has varying path delays and switching activity, the problem can be divided in two sub-problems: *A*) to group the pattern set into different subsets with very close pattern delay distribution and *B*) to find an optimum frequency for each group considering *faster-than-at-speed IR-drop* effects. Both will be discussed in the following sub-sections.

3.1 Pattern Grouping

The launch-off-capture transition fault pattern set (2803 patterns) was generated using Synopsys Tetramax [10]. Figure 8 shows the maximum path delay affected in each pattern. Note that each pattern can effect various endpoints, but we only considered the endpoint with the maximum delay (minimum slack) for each pattern. The functional operating cycle time period is represented by T=$7000ps$. It can be noticed that the affected paths in each of the pattern has considerable amount of slack for the small delay defects to escape during manufacturing test. This is because in most cases, the ATPG tools can always find a shorter path to activate and propagate the

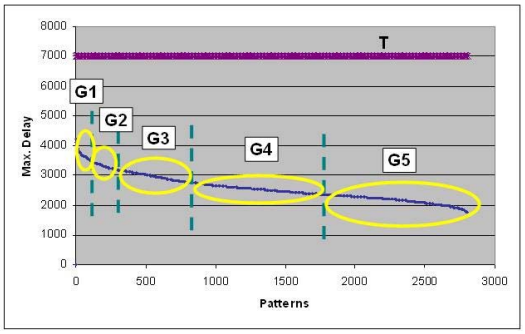

Figure 9: Sorted transition fault pattern set based on maximum path delay.

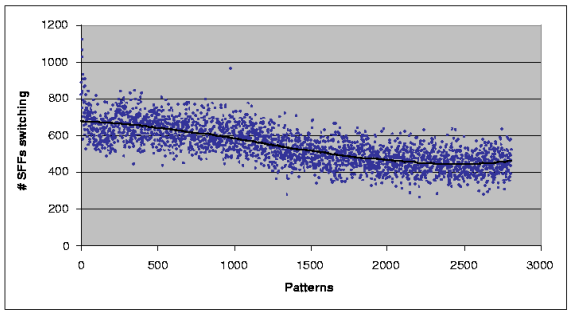

Figure 10: Number of switching scan flip-flops in each transition fault test pattern.

transition fault effect. However, techniques such as multiple-detect [14] and K-longest paths [8] can be applied at the expense of ATPG run-time, which forces the ATPG tool to search more paths in order to detect the same fault, thereby, increasing the chances of affecting longer paths.

Each transition fault test pattern has varying delay distribution and switching activity (related to IR-drop) and it is very difficult to perform detailed analysis of each pattern as explained in Section 2. However, even if such a detailed analysis was feasible, it may be difficult to apply each pattern at a different frequency. This might be either due to hardware limitations of the automatic test equipment (ATE) to generate multiple higher frequencies or due to the on-chip clock generators (phase locked loop (PLL)) limitation of long synchronization time.

In order to group the patterns with relatively close path delay distribution, the patterns are sorted in increasing order of *pattern slack*. We refer *pattern slack* as the least slack (maximum path delay) across all the endpoints in the respective pattern. Figure 9 shows the maximum path delay for each pattern in the resulting sorted pattern set. For faster-than-at-speed pattern application, the patterns with very close *pattern slack* distribution are grouped together (as shown in Figure 9). There are five groups $G1$ through $G5$ and the *pattern slack* range for each group was selected as $450ps$. Although, a more tight pattern slack range can be selected but it increases the number of groups and more processing will be required for IR-drop analysis for each group. Assuming a fixed faster-than-at-speed cycle time for each group, the first pattern in each group will have the least *pattern slack* and hence, it is used in determining the faster-than-at-speed test clock period for the respective group. If T'_{Gi} represents the new faster-than-at-speed clock period for a group then T'_{Gi} can be formulated as $T'_{Gi} = T_{Gi} + |\Delta T_{Gi}| + \tau_{su}$, where T_{Gi} represents the maximum path delay for pattern group i, ΔT_{Gi} represents the worst-case performance degradation due to *faster-than-at-speed IR-drop* of group Gi and τ_{su} is the setup time for the scan flip-flops.

3.2 Toggle Activity

To determine the optimal test clock period (T'_{Gi}) for each pattern group, it is required to measure the worst-case performance degradation (ΔT_{Gi}) for the pattern group, which is directly related to worst-case IR-drop. Alternatively, the IR-drop is related to the number of switching nets inside the circuit. Due to the large number of nets in the design and the random nature of switching activity for each test pattern, it is very difficult to estimate the IR-drop. Simulation-based techniques can be used to capture the switching activity information in the standard *value change dump (VCD)* format. But, this technique is sufficient only to analyze a very small number of patterns due to the extremely large size of VCD files for large designs.

To overcome this problem, we measure only the switching activity of the scan flip-flops using programming language interface (PLI) routines during gate-level verilog simulation. The PLI provides a standard interface to the internal data representation of the design during simulation. The switching activity among the scan flip-flops provides a good estimate of the number of switchings inside the circuit. For example, a pattern $P1$ with a large number of scan flip-flops switching is likely to have greater switching activity inside the circuit than a pattern $P2$ with a small number of scan flip-flops switching. Figure 10 shows the number of flip-flops switching in each transition fault test pattern during the launch and capture functional cycles of the launch-off-capture pattern. It can be noticed from the trend line (Figure 10) that the initial patterns have high scan flip-flop switching activity and the very gradually reduces. This is because the initial patterns detect most of the transition faults and the later patterns target the hard-to-detect faults. The above procedure using PLI interface avoids the VCD file generation for estimation of switching activity. However, the VCD file is still required for IR-drop analysis but it is performed only on one pattern in each group with the highest number of switching scan flip-flops.

After determining the pattern in each group with the maximum scan flip-flop switching activity, the entire net toggle activity for this particular pattern is captured in VCD file and the worst-case IR-drop analysis is performed. In the next step, the corresponding design timing information (SDF file) at the reduced voltage condition ($V' = V - V_{worst-IR-drop}$) will be applied to the least slack pattern in the group, to measure the worst-case performance degradation for the respective group.

4. EXPERIMENTAL RESULTS

We have developed a perl program which takes as input the maximum path delay and the scan flip-flop switching activity information for each pattern and divides the pattern set into different user-defined number of groups. The groups are divided based on the relative closeness of *pattern slack*. Here, we select the *pattern slack* range as $450ps$ to generate a reasonable number of pattern groups (5 groups in our case). However, this is configurable and decreasing the *pattern slack* range increases the number of pattern groups.

Table 1 show the results obtained for each group $G1$ through $G5$ after sorting the pattern set based on maximum path delay of each pattern. The worst-delay (T_{Gi}) of a group is the maximum delay of a pattern in each group (Column 3). To estimate the worst case average IR-drop in each group, a pattern with the maximum

Table 1: Results for different pattern groups for ITC'99 benchmark (*b19*).

Group	# Patterns	Worst-delay (T_{Gi})	Worst Avg. (ΔVDD_{IRdrop})	Worst Avg. (ΔVSS_{IRdrop})	Worst Performance degradation (ΔT_{Gi})[ps]	Faster-than-at-speed period ($T'_{Gi} = T_{Gi} + \Delta T_{Gi} + \tau_{su}$)
G1	29	4214	0.196	0.253	773	5187
G2	163	3764	0.193	0.252	871	4835
G3	469	3314	0.143	0.224	1056	4570
G4	939	2864	0.101	0.158	826	3890
G5	1203	2414	0.137	0.219	1146	3760

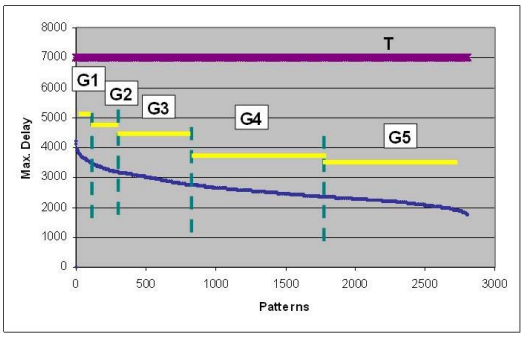

Figure 11: Transition fault pattern groups with their respective faster-than-at-speed clock period.

number of scan flip-flops switching was selected and an IR-drop analysis was performed as explained in Section 2. Columns 4 and 5 in Table 1 show the worst case IR-drop for VDD ($\Delta VDD_{IR-drop}$) and VSS ($\Delta VSS_{IR-drop}$), respectively.

In order to take into account the performance degradation effect due to *faster-than-at-speed IR-drop*, the design timing information at the respective effective voltage ($\Delta V = \Delta VDD_{IR-drop} + \Delta VSS_{IR-drop}$) was generated for each group. For example, in case of group $G1$, the effective voltage is $VDD - \Delta V = 1.8 - (0.196 + 0.253) = 1.35V$. In general, an ASIC technology library is characterized at multiple operating voltage conditions. In our case, we had characterized the standard cell library in decreasing steps of $0.1V$ using Synopsys NanoChar. Hence, for group $G1$ with effective voltage reduction of $\Delta V = 0.45V$, we selected the cell timing library at operating voltage $1.3V$ to generate the design timing information. This also provides a safe margin for un-accountable effects, such as process variation, etc. After generating the design information, the pattern with the maximum delay in the group is simulated to obtain the worst performance degradation due to *faster-than-at-speed IR-drop* (column 6 in Table 1). Finally, the resulting worst-case performance degradation is used to determine the *faster-than-at-speed* clock period ($T'_{Gi} = T_{Gi} + \Delta T_{Gi} + \tau_{su}$) for the respective pattern group. Figure 11 shows the original rated functional period and *faster-than-at-speed* clock timing for each of the group considering IR-drop effects. It can be noticed that there is extra slack provided by our technique between the maximum delay of the pattern group and the faster-than-at-speed clock period to take into account the performance degradation due to increase in IR-drop effects.

5. CONCLUSION

We have presented a detailed analysis of faster-than-at-speed techniques utilized for small delay fault detection. The analysis illustrated that the IR-drop is exacerbated during faster-than-at-speed pattern application (upto 16% compared to IR-drop at rated functional speed) and it is important to consider the performance degradation of the design due to increase in IR-drop effects. We have proposed a new framework for applying transition fault test patterns at faster-than-at-speed considering both the performance degradation due to adverse IR-drop effects and positive slack. The proposed technique groups the pattern set based on their affected maximum delay and determines the worst case performance degradation for each pattern group. This avoids false identification of good chips to be fault due to IR-drop effects rather than small delay defects.

6. REFERENCES

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