

ODOR: A Microresonator-based High-performance Low-cost Router for Optical Networks-on-Chip

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ABSTRACT

The performance of system-on-chip is determined not only by the performance of its functional units, but also by how efficiently they cooperate with one another. It is the on-chip communication architecture which determines the cooperation efficiency. Network-on-Chip (NoC) is introduced to improve communication bandwidth and power efficiency. However, traditional metallic interconnects consume significant amount of power to deliver large communication bandwidths. Optical NoCs are based on silicon optical interconnects with significant bandwidth and power advantages. Optical routers are the key enabling components of optical NoCs. This paper proposed a novel optical router architecture, ODOR, for optical NoCs based on XY routing algorithm. We compared ODOR with four other router architectures, and analyzed three aspects in details, including power consumption, optical power insertion loss, and the number of microresonators. The results show that ODOR has the lowest power consumption and losses and requires the least microresonators. ODOR has 40% less power consumption, 40% less loss, and 52% less microresonator than the full-connected crossbar. Furthermore, ODOR has a special feature which guarantees the maximum power to route a packet through a network to be a small constant number, regardless of the network size. The maximum power consumption is 0.96fJ/bit under current technology. We simulated a 6x6 2D mesh NoC based on ODOR, and showed the end-to-end delay and network throughput under different offered loads and packet sizes.

Categories and Subject Descriptors

C.1.2 [Processor Architecture]; C.5.4 [VLSI Systems];

General Terms: Performance, Design, Theory

Keywords: Network on chip, optical interconnect, router architecture, microresonator, low power, loss

1. INTRODUCTION

On-chip communications are facing new challenges in the billion-transistor system-on-chip (SoC) paradigm [1][2][3][4]. When the number of transistors in a single chip increases to billions or even

larger numbers, traditional on-chip communication techniques for SoC face several issues, such as poor scalability, limited bandwidth, low utilization, and so on [5][6][7]. Networks-on-chip (NoCs) promise to relieve these issues by modern communication and networking theories. Many NoCs have been proposed, such as Dally's NoC [8], SPIN [9], Nostrum [10], Æthereal [11], ASNoC [12] and etc. However, as semiconductor technologies continually scale the feature sizes down and the on-chip communications required by new applications increases, the conventional metallic interconnect is becoming the bottleneck of NoC performance with limited bandwidth, long delay, and high power consumption. Therefore, electronic NoC may not satisfy future bandwidth and latency requirement within the power consumption budget [13][14][22].

Optical NoC is based on optical interconnect and is a promising candidate to overcome these limitations. Before applied to NoC, optical interconnect has demonstrated its strengths in multicomputer systems [15], on-board inter-chip interconnect [16], and switching fabrics in core routers [17]. Wavelength-division multiplexing (WDM) technologies use multiple wavelengths to provide larger bandwidth than a single wavelength, and optical time-division multiplexing (OTDM) technologies help to improve network utilization. Optical networks use circuit-switching-like transmission mechanism. Once a connection is established, the communication latency can be guaranteed.

Optical routers are the key components of an optical NoC. Compared with electronic routers, optical routers are based on different switching principles and have different design constrains. For example, the basic switching elements in typical optical routers switch once for each packet instead of for each bit as in electronic routers. Different from metallic interconnects, optical waveguide crossings introduce non-negligible waveguide insertion loss. Recent progress in optical technologies, especially the development of microresonators, makes optical on-chip routers more realistic [18]. An optical microresonator is an integrated optical structure. It is a good candidate for very large scale integrated optoelectronic circuits. Microresonators can be fabricated on SOI substrate and is only 12 μm in diameter [19].

Several optical on-chip routers, which are based on microresonators, are proposed in literature. A non-blocking optical router based on a full-connected crossbar is proposed in [19]. Each port of the router is aligned to its corresponding direction to reduce the waveguide crossings. An optical router, λ -router, is proposed in [20]. λ -router is based on WDM technology and a passive switching fabric. An NxN router uses N wavelengths and multiple basic 2x2 switching elements to realize non-blocking switching function. The

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λ -router architecture prefers N to be an even number, so that all the components can be fully utilized. Another non-blocking router is proposed in [21]. It is based on a 2×2 switching element design to implement a 4×4 router. Since typical 2D NoCs use 5×5 routers, the 4×4 router is augmented by extra ports for local injection and ejection.

Dimension order routing algorithm has been favored by many NoC studies [23][24] [25][26][27], and is also called XY routing in 2D-mesh and 2D-torus networks. In XY routing, each packet is routed first in X dimension until it reach the node, which is in the same column with the destination, and then along the perpendicular Y dimension to the destination. XY routing is a minimal path routing algorithm and is free of deadlock and livelock. In addition, it is a low-complexity distributed algorithm without using any routing table. These features make XY routing algorithm particularly suitable for NoCs, which require low latency and low cost at the same time.

In this paper, we propose a new router, ODOR (Optical Dimension Order Router), for optical NoCs using XY routing algorithm. Compared with other routers, ODOR requires fewer microresonators, consumes less power, and has lower optical power loss. It has been designed to take advantages of the properties of XY routing. To save power and reduce optical power loss, the microresonators of an ODOR are active only when packets need to make turns. The ODOR architecture is presented in section 2. Detailed comparisons and analysis with other optical NoC routers is shown in Section 3. Section 4 analyzes the performance of a 2D mesh optical NoC using ODOR based on simulations. Section 5 concludes the paper.

2. ODOR ROUTER

Optical routers are the key components of an optical NoC. They implement the routing and flow control functions. An optical router switches packets from an input port to an output port using a switching fabric, which is composed of multiple basic switching elements.

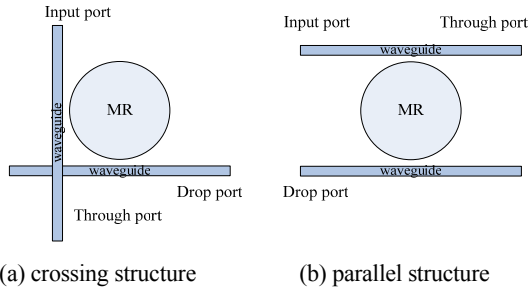


Figure 1. Structures of 1×2 switching elements using optical microresonators

2.1 Basic Switching Elements

ODOR is based on the optical microresonators. We use two structures, the crossing structure and parallel structure, to implement the basic 1×2 switching elements for ODOR, as shown in Figure 1. They both consist of two waveguides and one microresonator. The main difference is the positions of the waveguides. The microresonator has an off-state resonance wavelength λ_{off} when the microresonator is powered off. λ_{off} is determined by the material and internal structure of the microresonator. The switch time of the microresonator is small, and a 30ps switching time has been

demonstrated [28]. When the microresonator is powered on, the resonance wavelength changes to the on-state resonance wavelength λ_{on} . The advantage of the parallel structure over the crossing structure is that there is no waveguide crossing insertion loss. If the wavelength of an optical signal is different from the resonance wavelength, it will be directed to the through port. Otherwise, the signal will be routed to the drop port. By powering on or off the microresonator, the basic switching elements can be controlled to switch a packet to either the drop port or through port.

2.2 Traditional and Reduced Crossbars

The switching fabric of an optical router architecture can be implemented using the traditional full-connected crossbar. An $N \times N$ optical router requires an $N \times N$ crossbar, which is composed of N^2 microresonators and $2N$ crossing waveguides. Figure 2 (a) shows a 5×5 full-connected crossbar, which has the injection port and ejection port for traffics from and into a local tile besides four input ports and four output ports for each direction.

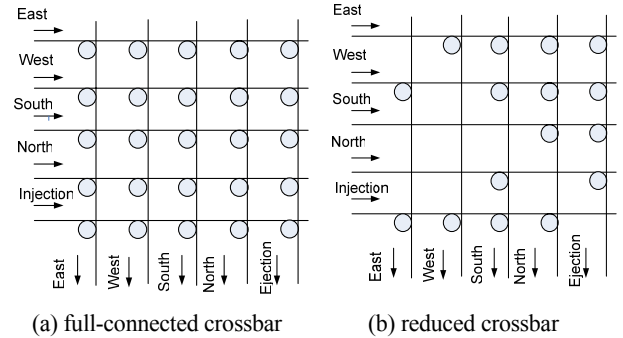


Figure 2. Traditional 5×5 crossbar switching fabrics

The full-connected crossbar can be reduced for XY routing algorithm, because some turns are not required. For example, a packet will not make turns from south to east according to XY routing algorithm. Moreover, since U turns are not allowed, the turns that from one direction to itself can also be omitted. Figure 2 (b) shows a 5×5 reduced crossbar topology for the networks using XY routing algorithm. Compared with the full-connected crossbar, the 5×5 reduced crossbar saves nine microresonators, but has the same number of waveguide crossings. It does not improve the loss or power consumption over the traditional crossbar.

2.3 ODOR Architecture

We proposed a new optical router architecture, ODOR (Optical Dimension Order Router), for optical NoCs based on XY routing algorithm. ODOR architecture is shown in Figure 3. It consists of a switching fabric and a control unit which uses electrical signals to configure the switching fabric according to the routing requirement of each packet. The switching fabric includes the input demultiplexers (DEMUXs), the ejection multiplexer (MUX), and the switching core. The microresonators (MRs) in the input demultiplexers and switching core are identical, and have the same on-state and off-state resonance wavelengths, λ_{on} and λ_{off} . ODOR uses a single wavelength which corresponds to λ_{on} .

There is an input demultiplexer for each input port of the four directions (East, North, West, and South). The demultiplexer is built from the basic 1×2 switching element, and uses the parallel structure to avoid waveguide crossing insertion loss. It separates the packets whose destinations are the current tile from those who pass through the current router. When a packet arrives at an ODOR router, if its

destination is the current tile, it will be directed to the ejection multiplexer without entering the switching core; otherwise, it will be directed to the switching core where it is switched to one of the four directions. This separation scheme reduces the traffic entering the switching core and the complexity of the switching core. To reduce the worst-case accumulated insertion loss in a network, the drop ports of the 1x2 switching elements are connected to the ejection multiplexer.

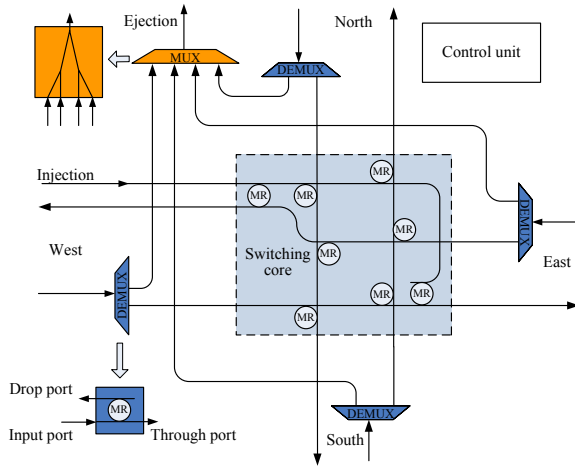


Figure 3. ODOR architecture

Since at any given clock cycle, only one input of the ejection multiplexer may have packets to be ejected into the current tile, only a passive multiplexer is required. The passive multiplexer uses three Y branches. Each Y branch has a $14 \times 8 \mu\text{m}^2$ footprint and 0.3dB loss [29]. An alternative design uses three active microresonators. Compared with the alternative design, our design has less insertion loss, no control wires, and zero power consumption.

The switching core implements a 5x4 switching function, and the full 5x5 switching function of ODOR router is implemented with the help of the input demultiplexers and ejection multiplexer. The switching core uses only eight microresonators and five waveguides. We can also replace the last microresonator on the waveguide for the injection port with a Y branch. Although this reduced the number of microresonators and save power, more loss will be encountered by packets which exit from the east port. Compared with the crossbars, it uses not only the basic 1x2 switching elements with the crossing structure, but also those with the parallel structure to reduce the waveguide crossing insertion loss. Furthermore, the internal structure of the switching core is designed to avoid waveguide crossings. Both the switching core and input demultiplexers are controlled by the control unit. The control unit is built from traditional CMOS transistors and uses electrical signals to power on and off each microresonator according to the routing requirement of each packet. The control units of all the ODOR routers in an optical NoC use an electronic network to setup and maintain optical paths.

ODOR architecture has an excellent feature. Regardless of the network size, the maximum power to route a packet through a 2D NoC based on ODOR is a constant number. As we will see in the following section, the constant number is very small and close to the average power consumption. This feature is especially helpful for large networks and network scalability. The feature is designed by

avoiding any microresonator switching activity for routing packets between the two horizontal ports and the two vertical ports in the ODOR architecture. This means that at most three ODOR routers need to power on one microresonator each for any packet in a network of any size.

For optical NoCs using XY routing algorithm, ODOR router is strictly non-blocking. This can be proved by listing all the possible cases. For example, when a packet is injected from injection port to the east port, it will not block packets from west to south, or west to north, or south to north, or north to south. Some cases are not allowed by XY routing algorithm, such as that turns from south/north to east/west.

3. COMPARISON AND ANALYSIS

We compared the ODOR architecture with the other four optical router architectures including the λ -router, full-connected crossbar, reduced crossbar, and router architecture proposed in [21], which is referred to as CR for clarity. We compared and analyzed three main aspects of the above router architectures, including the power consumptions, optical power insertion losses, and numbers of microresonators. Since NoCs using regular 2D topology require 5x5 routers and the λ -router architecture supports the even number of input and output ports, a 6x6 λ -router is used in the comparison with one pair of idle input and output ports.

The number of microresonators used by an optical router decides its area cost along with its floorplan. Lower number of microresonators indicates a lower chip cost by reducing die size and increasing yield. We compared the numbers of microresonators required to implement the five optical router architectures. ODOR uses the lowest number of microresonators, 12, which is 52% less than the full-connected crossbar (Figure 4). Compared with ODOR, the reduced crossbar uses just four more microresonators, but its power consumption and optical power losses are much higher as we will see. λ -router requires the highest number of microresonators mainly due to the multistage switching structure. Full-connected crossbar has the second largest number of microresonators. CR also requires a relative large number of microresonators because of the additional gateway accessing points to implement the 5x5 switching function. As for the ODOR architecture, the switching core only uses eight microresonators in addition to the four microresonators used by the input multiplexers for the directions.

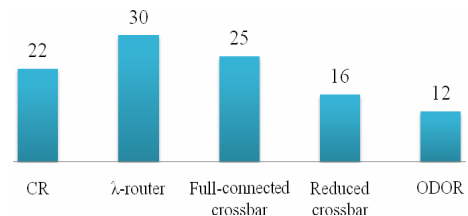


Figure 4. Numbers of microresonators

Power consumption is a critical aspect of optical NoC design. For high-performance computing, low power consumption can reduce the cost related with packing, cooling solution, and system integration. Optical NoCs consume power in three ways. First, optical NoC interfaces consume power to generate, modulate, and detect optical signals. Second, optical routers consume power to route packets. Third, the networked control units of an optical NoC consume power to communicate and process routing information. We are concentrated on the second item and assume the five routers use the same networked control units and network interfaces for XY

routing algorithm. Since the λ -router uses WDM and a passive switching fabric, it requires extra units for wavelength selection or conversion, which the authors did not reveal the design details. Due to incomplete information, we could not compare the power consumption of λ -router with other routers.

Due to the asymmetrical architecture of an optical router, a packet taking different input and output ports will require different amount of power to route it. To better measure the power efficiency of the optical routers, we analyzed the average power consumption of a router in the 6x6 2D mesh NoC. The average power consumption E is calculated using the equation (1). M is the total number of paths in a network. E_i is the power consumed on the i -th path when the bandwidth is B . R_i is the number of routers on the i -th path.

$$E = \frac{\sum_{i=1}^M \frac{E_i}{R_i}}{M \times B} \quad (1)$$

We assume a moderate bandwidth of 12.5Gbps for each path in the network. An optical router needs to power on and off its microresonators to route packets. In the on state, the microresonator need a DC current and consume less than 20 μ W [19]. In the off-state, no power will be consumed by a microresonator, if we ignore the small bias voltages to mitigate process variations. The power consumption of the microresonator is expected to decrease with continual improvement of its material and internal structure.

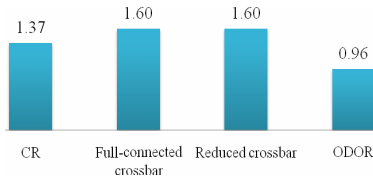


Figure 5. Average power consumption (fJ/bit)

The comparison result shows that ODOR has the lowest average power consumption, 0.96fJ/bit, which is 40% less than the two crossbar architectures. A further analysis shows that the maximum power consumption of ODOR in the network is also 0.96fJ/bit. This coincidence is due to most packets in a network based on ODOR needs the same amount of power to route and the limited precision of the two numbers hides the small difference. Regardless the size of a network, ODOR has a constant maximum power consumption, thanks to the optimized architecture. This can be proved as follows. According to the architecture, ODOR does not need to power on any microresonator for a packet traveling along a column or row. ODOR only powers on one microresonator when a packet enters a network from an injection port, turns from a row to a column, or exits the network from an ejection port. In the worst case, at most three microresonators are powered on to route a packet in a network based on ODOR, and this number does not change with the network size. This feature allows an optical network based on ODOR scales without worrying the power consumed by the additional routers on a longer path. In comparison, a network based on the other routers does not scale well.

Optical power losses of an optical NoC decide its feasibility as well as the power consumption required by the NoC interfaces to generate, modulate, and detect optical signals. In our comparison, we considered two major sources of optical power losses, the waveguide crossing insertion loss and microresonator insertion loss. The waveguide crossing insertion loss is 0.12dB per crossing [19],

and the microresonator insertion loss is 0.5dB [32]. Since the waveguides can be fabricated on different layers to avoid crossing [30], we only consider the waveguide crossings inside switching core which are hard to avoid. The waveguide propagation loss is only 0.17dB/mm [22], and we omit it because all the routers are compared in the same NoC.

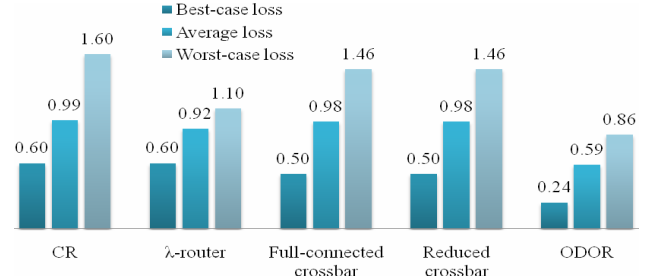


Figure 6. The best-case, worst-case, and average losses (dB)

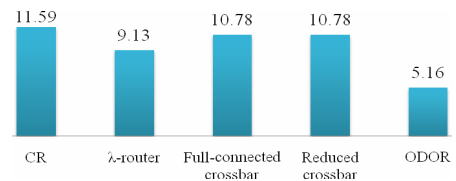


Figure 7. Average longest path loss (dB)

Different input-output pairs of an optical router may have different losses. We compared the worst-case loss, best-case loss, and average loss of all possible cases (Figure 6). The ODOR architecture has the lowest losses in all the categories. ODOR has 52% less best-case loss, 40% less average loss, and 41% less worst-case loss than the two crossbar architectures. We also compared the average loss of the longest paths in the 6x6 2D mesh NoC (Figure 7). ODOR still has the lowest loss in this comparison, which is 5.16dB, while the two crossbars have the highest loss. ODOR has 52% less average longest path loss than the full-connected crossbar.

4. SIMULATION RESULTS

We built a 6x6 2D mesh optical NoC using ODOR and XY routing algorithm, and studied its performance (Figure 8). The optical NoC consists of two overlapped networks, an optical network for large payload packets and an electronic network for control packets and small payload packets. Payload packets carry data and processor instructions, while control packets carry the network control information. The electronic network connects the control units of all the ODOR routers in the same topology as the optical network. In general, the topologies of the two networks can be different. For example, torus can be used for the optical network by adding a waveguide to each pair of end routers. The optical and metallic interconnects are all bidirectional. While the optical interconnects are 1-bit wide on each direction, metallic interconnects are 32-bit wide on each direction. In the optical NoC, processors generate packets independently and at time intervals following a negative exponential distribution. We used the uniform traffic pattern, i.e. each processor sends packets to all other processors with the same probability. The optical NoC is simulated using a network simulator, OPNET [31]. We assumed a moderate peak bandwidth, 12.5Gbps, for each injection port. 12.5Gbps can be achieved by using a single modulator based on microresonators [28].

The performance of the optical NoC is measured in terms of end-to-end (ETE) delay and throughput. The ETE delay is the average time between processors generating packets and the packets reaching destinations. It is the sum of the connection-oriented path-setup time and the time used to transmit optical packets. The throughput of the optical NoC measures the total throughput of the network under a given offered load. Offered load α can be calculated as in equation (2).

$$\alpha = \frac{T_{transmission}}{T_{transmission} + T_{gap}} \quad (2)$$

$T_{transmission}$ is the time that a network spend to transmit packets, and T_{gap} is an exponentially distributed time between two packets. We simulated a range of packet sizes used by typical SoC applications, and use the 32-bit size for path-setup and acknowledge packets.

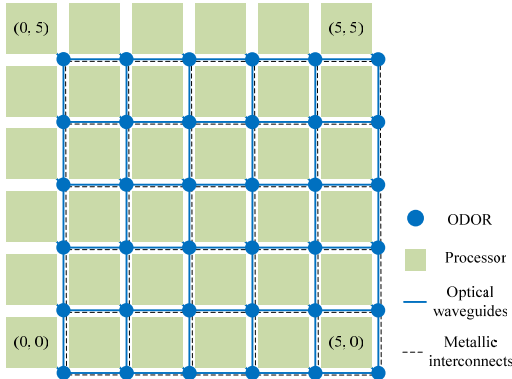


Figure 8. A 6x6 2D mesh NoC based on ODOR

The ETE delay under different offered load is shown in Figure 9. The network saturates at different loads with different packet sizes. The ETE delay is very low before the saturation load, and increases dramatically after it. For the 8B packets, ETE delay is 30ns before the saturation load 0.07, and goes up to 7 us after the saturation load. Packets larger than 8B have much higher saturation load. In XY routing algorithm, each payload packet corresponds to two control packets, one path-setup packet and one acknowledge packet. Under the same offered load, larger packets cause the network to use less control packets compared with smaller packets. Larger packets also have longer transmission times and cause longer inter-packet arrival gaps compared with smaller packets under the same offered load. Long inter-packet arrival gaps can reduce network blocking during path setup. The combined effect makes larger packets suffer from less congestion, and hence have higher saturation loads than smaller packets. As the packet size increases, the difference between the ETE delay curves of adjacent packet sizes becomes smaller. The balance point is decided by the mesh topology, XY routing algorithm, and traffic pattern. Figure 10 shows the network throughput under different offered load using the different packet sizes. The trend concluded from ETE delay can be obtained more clearly here.

5. CONCLUSION

We proposed a novel optical router architecture, ODOR (optical dimension order router), for optical NoCs which use XY routing algorithm. The paper compared ODOR with four other router architectures. The comparison results show that ODOR has the lowest power consumption and losses and requires the least microresonator. For example, ODOR consumes 40% less power,

has 40% less loss, and requires 52% less microresonator than the full-connected crossbar. ODOR can guarantee the maximum power to route a packet through a network to be a small constant number, regardless of the network size. The number is 0.96fJ/bit under current technology. Furthermore, the maximum power consumption is very close to the average power consumption. We simulated a 6x6 2D mesh NoC based on ODOR and XY routing algorithm, and showed the end-to-end delay and network throughput under different load and packet sizes, which are typically used in SoC applications.

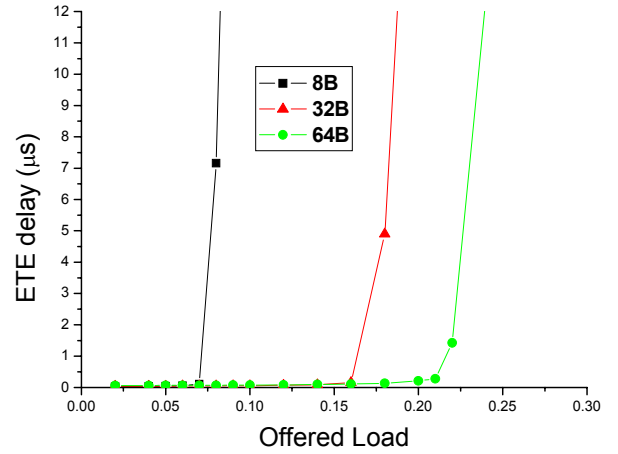


Figure 9. ETE delay vs. offered load

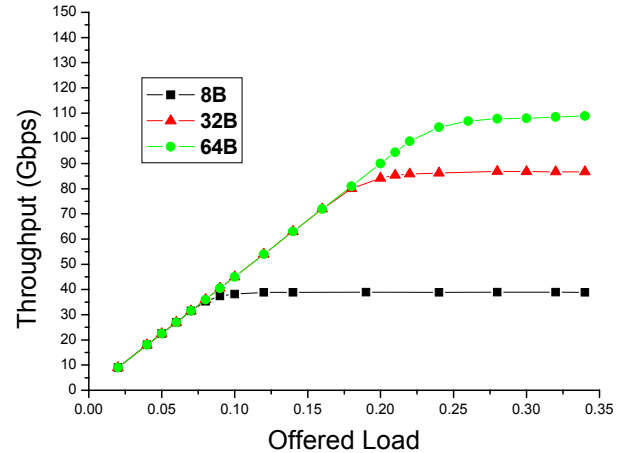


Figure 10. Throughput vs. offered load

6. ACKNOWLEDGMENT

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REFERENCES

- [1] L. Benini and G. De Micheli, "Networks on chip: A new paradigm for systems on chip design", *Design, Automation and Test in Europe Conference and Exhibition*, 2002.

- [2] M. Sgroi, M. Sheets, A. Mihal, K. Keutzer, S. Malik, J. Rabaey, and A. Sangiovanni-Vincentelli, "Addressing the system-on-a-chip interconnect woes through communication-based design", *Design Automation Conference*, 2001.
- [3] G. Martin, "Overview of the MPSoC design challenge", *Design Automation Conference*, 2006.
- [4] S. Ogg, E. Valli, C. D'Allesandro, A. Yakovlev, B. Al-Hashimi, and L. Benini, "Reducing Interconnect Cost in NoC through Serialized Asynchronous Links", *In Proc. of 1st ACM/IEEE International Symposium on Networks-on-Chip*, 2007.
- [5] D. Shin, A. Gerstlauer, R. Dömer, and D. D. Gajski, "Automatic network generation for system-on-chip communication design", *CODES+ISSS 2005*, pp255-260.
- [6] J. Henkel, W. Wolf, and S. T. Chakradhar, "On-chip networks: A scalable, communication-centric embedded system design paradigm", *in Proc. 17th International Conference on VLSI Design*, 2004.
- [7] W. Wolf and A. A. Jerraya, "Application-Specific System-on-a-Chip Multiprocessors", *IEEE Design & Test of Computers*, Vol.18, No.5, pp7- , 2001.
- [8] W. Dally and B. Towles, "Route packets, not wires: On-chip interconnection networks", *Design Automation Conference*, 2001.
- [9] P. Guerrier, A. Greiner, "A generic architecture for on-chip packet-switched interconnections", *In Proc. of the Design Automation and Test in Europe (DATE)*, pp250-256, 2000.
- [10] S. Kumar, A. Jantsch, J.P. Soininen, M. Forsell, M. Millberg, J. Öberg, K. Tiensyrjä, and A. Hemani, "A network on chip architecture and design methodology", *IEEE Computer Society Annual Symposium on VLSI*, 2002.
- [11] K. Goossens, J. Dielissen, A. Radulescu, "Æthereal network on chip: Concepts, architectures and implementations", *IEEE Design Test Computer*, Vol.22, No.5, pp414-421, 2005.
- [12] J. Xu, W. Wolf, J. Henkel, and S. Chakradhar, "A Design Methodology for Application-Specific Networks-on-Chip", *ACM Transactions on Embedded Computing Systems*, July 2006.
- [13] J. Fujikata, K. Nishi, A. Gomyo, et al, "LSI On-Chip Optical Interconnection with Si Nano-Photonics", *IEICE Transactions on Electronics*, Vol.91-C, No.2, pp131-137, 2008.
- [14] A. Driessen, D. H. Geuzebroek, and E.J. Klein, "Optical network components based on microring resonators", *In proc. of 8th International Conference on Transparent Optical Networks*, pp. 210-215, 2006.
- [15] R.D. Chamberlain, M.A. Franklin, and Ch'ng Shi Baw, "Gemini: An Optical Interconnection Network for Parallel Processing", *IEEE Transactions on Parallel and Distributed Processing*, Vol. 13, No. 10, pp1038-1055, 2002.
- [16] M. P. Christensen, P. Milojkovic, M.J.McFadden, and M.W. Haney, "Multiscale optical design for global chip-to-chip optical interconnections and misalignment tolerant packaging", *IEEE Journal of Selected Topics in Quantum Electronics*, Vol.9, No.2, pp. 548-556, 2003.
- [17] J. Gripp, M. Duell, J.E. Simsarian, A. Bhardwaj, P. Bernasconi, O. Laznicka, M. Zirngibl, "Optical switch fabrics for ultra-high-capacity IP routers", *Journal of Lightwave Technology*, Vol.21, No.11, pp. 2839-2850, 2003.
- [18] Q. Xu, B. Schmidt, S. Pradhan, and M. Lipson, "Micrometre-scale silicon electro-optic modulator", *Nature*, Vol.435, No.7040, pp325-327, 2005.
- [19] A. W. Poon, F. Xu, X. Luo, "Cascaded active silicon microresonator array cross-connect circuits for WDM networks-on-chip", *in Proc. SPIE Int. Soc. Opt. Eng.* 6898, 689812 (2008).
- [20] M. Briere, B. Girodias, et al, "System Level Assessment of an Optical NoC in an MPSoC Platform", *Design, Automation & Test in Europe Conference & Exhibition*, 2007.
- [21] A. Shacham, B.G. Lee, A. Biberman, K. Bergman, and L.P. Carloni, "Photonic NoC for DMA Communications in Chip Multiprocessors", *Hot Interconnects*, 2007.
- [22] F. Xia, L. Sekaric, and Y. Vlasov, "Ultracompact optical buffers on a silicon chip," *Nature Photonics*, 65-71, 2007.
- [23] J. Xu, W. Wolf, S. Chakradhar, and J. Henkel, "H.264 HDTV Decoder Using Application-Specific Networks-on-Chip", *IEEE International Conference on Multimedia and Expo*, July 2005.
- [24] M. Majer, C. Bobda, A. Ahmadinia, and J. Teich, "Packet Routing in Dynamically Changing Networks on Chip", *in proc. of 19th IEEE International Symposium on Parallel and Distributed Processing*, 2005.
- [25] J. Hu and R. Marculescu, "Energy-aware mapping for tile-based NoC architectures under performance constraints", *In Proc. ASP-DAC*, pp233-239, 2003.
- [26] G. Michelogiannakis, D. Pnevmatikatos, and M. Katevenis, "Approaching Ideal NoC Latency with Pre-Configured Routes", *in proc. of First International Symposium on network on chip*, pp.153-162, 2007.
- [27] J. Hu, U.t Y. Ogras, R. Marculescu, "System-Level Buffer Allocation for Application-Specific Networks-on-Chip Router Design", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 25, No. 12, pp2919-2933, 2006.
- [28] Q. Xu, S. Manipatruni, B. Schmidt, J. Shakya and M. Lipson, "12.5 Gbit/s carrier injection-based silicon microring silicon modulators", *Optics Express*, Vol.15, No.2, pp430-436, 2007.
- [29] E.Cassan, S.Laval, S. Lardenois and A. Koster, "On-chip optical interconnects with compact and low-loss light distribution in silicon-on-insulator rib waveguides", *IEEE Journal of Selected Topics in Quantum Electronics*, Vol.9, No.2, pp. 460-464, March-April 2003.
- [30] T. Hanai, S. Suzuki, Y. Hatakeyama and Y. Kokubun, "Vertically coupled microring resonator filter with multilevel crossing busline waveguide", *Jap. J. Appl. Phys.* 43, pp. 5785-5790, 2004.
- [31] www.opnet.com.
- [32] S. Xiao, M. H. Khan, H. Shen, and M. Qi, "Multiple-channel silicon micro-resonator based filters for WDM applications," *Optics Express*, vol. 15, pp. 7489-7498, 2007.