Bridging Gap between Simulation and Spreadsheet Study

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ABSTRACT
System architects working on SoC design have traditionally been hampered by the lack of a cohesive methodology for architecture evaluation and co-verification of hardware and software. This paper focuses on a comprehensive analysis framework providing platform assembly facilities, system analysis tools, enhanced traffic model and SystemC TLM IP. This framework has been intensively used to design and analyze complex SOC Interconnect based on STBus protocol such as the one of 71xx families. By hiding the complexity of a simulation and filling the gap towards spreadsheet study and costly On-Chip analysis using traffic model, architects benefit from an easy access to an efficient simulation for performance evaluation.

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General Terms: Performance, Verification.

Keywords: Performance, SoC, SystemC, Verification.

1. INTRODUCTION
Defining a SoC architecture and micro-architecture that will sustain the real-time constraints of the targeted applications is a great challenge. Assuming that every single IP of a SoC is sustaining its real-time constraints, the architecture/ micro-architecture definition and verification with respect to its performance will focus on the following critical components: Communication structure (including First In First Out to access the communication backbone) and Shared memory The architects will then need to define the following nformation

- IP Traffic Characterisation: Every IP in the SoC must be modelled in terms of the traffic.
- Application Real-time Constraints

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2. METHODOLOGY
The proposed methodology intend to bridge the gap between spreadsheet study of the application constraints and the simulation environement. Assuming that Architects will prefer study at a spreadsheet level such as Excel, but searching for accuracy, the environement proposed to the Architects should stay in Excel but results should be provided per accurate simulation.. To proceed the following elements has been designed:

- Intellectual Property Traffic Generator (IPTG): IPTG reads a configuration file describing an IP in terms of its traffic in order to re-generate the corresponding traffic on the communication backbone
- Memory Sub System (MSS): MSS models the communication backbone and memory controller and it is used in the analysis phase to define the communication micro-architecture features such as topology, arbitration, and FIFO size.
- Analysis Tool (AT): Analyze the simulated system and provides synthetic results which are related to the application constraints.

IPTG and AT being SystemC, whereas MSS can be refined from TLM to RTL implementations.

3. BRIDGING THE GAP
Using these three components the Architects will have access to an easy and powerfull environement. Allowing to focus only on filling IPTG and exploiting result inside Excel without knowing that results are generated from SystemC [1] platform (see Figure 1). A predefined Excel template allow the Architects to characterize each IP in terms of traffic and synchronization. Spreadsheet is then translated inside configurations file. Those configurations command the IPTG which has been instanciated to the MSS using SPIRIT [2] tools. During the simulation the Analysis tools will collect all system interaction and send it back to Excel. Consequently the architects continue to iterate only in their traditionnal spreadsheet environement. During the design flow, some of the MSS and IPTG will be refine through the RTL, allowing to verify the traffic model defined per the IPTG.

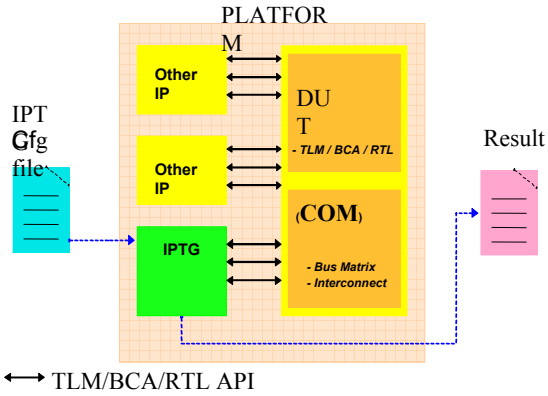

Figure 1: SystemC platform using IPTG and MSS

4. CONCLUSIONS

Allowing architects to bridge the gap between a paper and a simulation study is a first step. But still MSS and platform creation cannot be created and refine through Excel. IP-XACT standard from SPIRIT and according generators will allow to fill this new gap of automatically provide platform to architects. Automatic iteration through generators will natively be available.

5. ACKNOWLEDGMENTS

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6. REFERENCES

[1] www.systemc.org
[2] www.**spiritconsortium**.org