Power Deregulation: Eliminating Off-Chip Voltage Regulation Circuitry From Embedded Systems

Seunghoon Kim
Mobile Handset R&D Center
LG Electronics
Seoul, Korea 153-801
romuald@lge.com

Robert P. Dick, Russ Joseph
EECS Department
Northwestern University
Evanston, IL 60208, USA
(dickrp, rjoseph) ece.northwestern.edu

ABSTRACT

In battery-powered embedded systems, dedicated circuitry is used to convert stored energy into a form that can be directly used by processors. These power regulation devices seek to mask non-ideal aspects of the battery and present an ideal, fixed-voltage power source to the processor. However, this comes at a high price in terms of form factor, component cost, and energy efficiency. We describe and evaluate a new method for eliminating voltage regulation circuitry from battery-powered embedded systems. This method makes use of power gating, frequency scaling, and thread migration in chip-level multiprocessors to dynamically adjust to varying battery voltage. The key advantages of this approach are reduction in printed circuit board area (by 1/3 in many embedded applications) and the elimination of bulky unreliable discrete components such as electrolytic capacitors while maintaining similar battery lifespan. We have evaluated the power consumption, performance, and reliability implications of the proposed method using analytical techniques, power models, and detailed full-system simulation of numerous benchmarks from the ALPBench and MediaBench benchmark suites. For a number of battery technologies, the proposed technique holds the potential to eliminate power regulation circuitry and maintain battery lifespan while maintaining the same performance as systems using Buck-Boost voltage regulators.

Categories and Subject Descriptors: C.1.4 [Processor Architectures]: Parallel Architectures, Mobile processors; C.3 [Computer System Organization]: Real-time and embedded systems

General Terms: Design, Algorithms, Performance

1. INTRODUCTION

While mobile embedded system design has traditionally focused on techniques that optimize battery life or performance given a finite energy source, it has historically been dependent on low-level regulation circuitry to mask non-ideal behavior of the energy source. For example, batteries have load and time dependent characteristics that have required bulky, lossy regulators to present a clean, reliable, and well-controlled voltage to the processor. The presence of these components is generally assumed early during design, yet they often impose great cost. This cost has historically been ignored by due to the assumption that external power regulation circuitry is the only way to use non-ideal energy sources.

This work was supported in part by the NSF under awards CNS-0347941, CCF-0541337, and CNS-0720820.

CODES+ISSS'07, September 30–October 3, 2007, Salzburg, Austria.

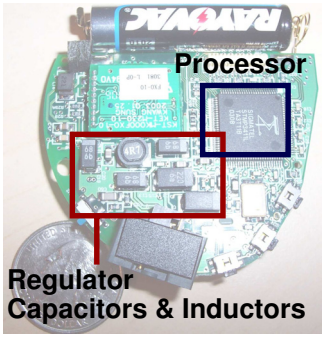

Figure 1: PCB for a MP3 audio player.

1.1 Power Regulation Overhead and Costs

Dedicated regulation circuitry may consume a significant amount of printed circuit board (PCB) area, leading to greater embedded system cost, weight, and size. For mobile devices, compactness, performance, and long battery life are frequently required. The bulk imposed by voltage regulators can make the difference between market share and failure. For a typical handheld media player, power regulation imposes a PCB area penalty of 600–718 mm^2 and a price penalty of $12.71. For example, power regulation circuitry accounts for over one-third of the total PCB area of typical media players such as the SONICBlue Rio MP3 shown in Figure 1. For an ordinary system setup with high-efficiency voltage regulation, such as Linear Technology's LTC3713 low input voltage DC–DC converter [1], the area cost of discrete components is approximately 718 mm^2. Techniques such as voltage regulation introduce substantial inefficiency. Step-down DC–DC converters, which are typically used in mobile systems, have conversion efficiencies around 85% [1].

Regulation circuits often include numerous unreliable discrete components that cripple the system if they fail. For example, the Apple iPod contains a power management IC, a voltage regulator IC, as well as surface-mount inductors, capacitors, and resistors. Many of these components are known to have high failure rates. Dell Inc. recently spent $300 million to correct long-term reliability problems caused by degradation of electrolytic capacitors [2].

1.2 Summary and Contributions

In this work, we introduce *Power Deregulation*, a design paradigm that eliminates board-level power regulation circuitry. We compensate by leveraging co-operative hardware–software management that can counteract non-ideal battery characteristics. Specifically, we scale the parallelism used to execute multithreaded workloads, e.g., multimedia applications, to match gradually-declining battery voltages. In today's mobile systems, energy source parameters (including voltage levels) change relatively slowly with respect to processor performance level (operating frequency), allowing operating systems and processors to adapt to evolving battery behavior.

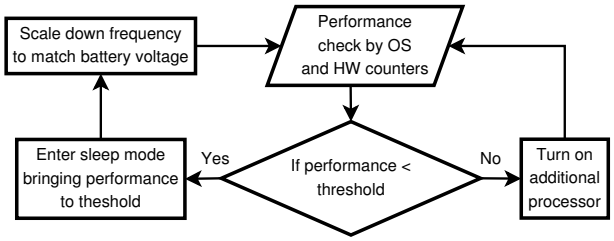

Figure 2: Power Deregulation procedure.

This is the first work to propose using dynamic chip multiprocessor (CMP) core activation and frequency scaling to adapt to voltage reduction during battery use. In contrast to conventional dynamic voltage frequency scaling (DVFS) approaches, we forego DC–DC voltage conversion. This prevents us from directly selecting a voltage/frequency operating point, but we compensate by scaling parallelism appropriately. By avoiding the regulation circuitry, we reduce the PCB size by approximately 30% and eliminate voltage regulator energy overhead which is commonly 85% for standard buck converters [1]. Our technique leverages chip multiprocessors, but is not the sole motivation for CMPs in the embedded domain; multi-core processors are seeing increasing use in embedded applications due to their good power efficiency, e.g., recent Apple iPods use dual core ARM processors. This trend is likely to continue in the future [3]. We have used detailed multiprocessor simulation to evaluate the performance and power consumption impacts of the proposed technique for numerous multimedia and pattern recognition applications. For embedded systems containing CMPs, the proposed technique is capable of significantly reducing embedded system PCB area and eliminating unreliable discrete components while maintaining the same performance as a regulated system. Battery lifespans are generally similar with or without the technique. For some battery technologies, Power Deregulation increases battery lifespan.

2. RELATED WORK AND BACKGROUND

Deregulated CMPs require scheduling and process migration in order to adapt to varying output battery voltages. This work builds on dynamic voltage and frequency scaling techniques [4, 5, 6, 7, 8]. Numerous existing embedded systems operate directly from raw battery outputs without voltage regulation, many popular sensor network nodes [9]. For example, the Telos ultra low-power wireless node [10] uses unregulated MSP430 RISC processors [11]. By using a clock frequency that provides great timing slack at high operating voltages, operation can continue during most of the useful life of the battery. These processors also incorporate monitors permitting software to react to long-term changes in battery voltage. The technique proposed in this paper builds on a concept long known to embedded systems designers: careful design in which both processor and power supply are considered can sometimes eliminate the need for voltage regulation circuitry. However, existing unregulated embedded systems rely on uniprocessors with performance margins large enough to maintain acceptable performance even when underclocked, thereby imposing tight limitations on performance or resulting in short battery lifespans. The proposed Power Deregulation technique exploits increasingly-prevalent multi-core processors to permit superior power and performance.

3. POWER DEREGULATION

In the proposed Power Deregulation technique, a processor is attached directly to the battery. This results in form factor and efficiency improvements. However, removal of power supply regulation circuitry complicates the problem of matching computational resources to their energy supplies. Embedded systems using

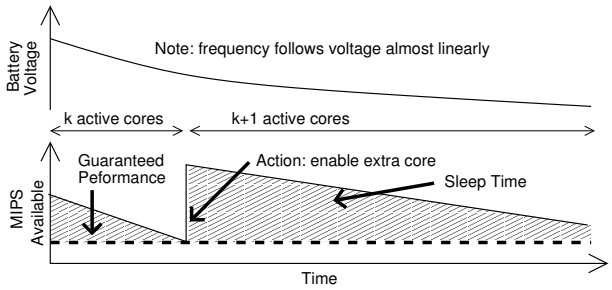

Figure 3: Activation of additional processors.

the proposed technique must respond to changing power supply voltage while continuously providing adequate performance. Figure 9 illustrates a typical battery discharge curve; voltage decreases with time, i.e., energy use, thereby increasing combinational path delay. In order to maintain reliable operation during battery discharge, operating frequency must progressively decrease. We assume the presence of on-chip voltage sensors that can dynamically adjust clock frequency in response to very slowly reducing battery voltage [8, 12, 13, 14]. As battery voltage declines, so does single-thread performance. We compensate by progressively activating additional processor cores, thereby increasing available thread-level parallelism.

Figures 2 and 3 outline power deregulation and provide a conceptual time line for a deregulated system. Peak performance decreases as battery voltage decreases; to compensate, deregulation enables additional processor cores and redistributes computation. This allows a deregulated system to maintain a constant level of performance without a voltage regulator. Following activation of additional cores, there may be surplus instruction throughput capacity to service tasks in the system. Allowing the processor cores to remain fully powered during these idle periods would be wasteful. Consequently, deregulation uses sleep modes to improve energy efficiency, as shown in Figure 3. Sleep modes are low-power states that can be used to reduce power consumption during time periods when computation is not required. As the battery depletes, voltage and frequency slowly decrease, increasing the time needed to complete a given task. This reduces the available sleep period. This process continues until there is no remaining slack and at this point another processor must be activated.

In this work, we set the performance requirement to 85% of a single processor core at its maximum frequency. In general, this performance tolerance can be adjusted based on workload properties and overall design goals. Whenever performance approaches this required level, the operating system activates an additional processor core to compensate. Operating system thread migration is used to distribute the workload appropriately. Note that battery voltage decreases gradually ($\sim$0.5 mV/s) as energy is consumed.

The fundamental difference between our approach and the passive dynamic frequency scaling implemented in ultra-low power systems like Telos is that we *enable additional cores to compensate* for performance that would otherwise be lost due to the declining battery voltage. Consequently, we can maintain the performance of a single core at peak frequency even when the battery is near its cutoff voltage. We anticipate that deregulation will be effective in systems that have more stringent performance demands than those of Telos class nodes.

Note that while deregulation removes conversion hardware otherwise dedicated to digital components, it cannot eliminate power regulation related to analog components. These analog components are sensitive to noise and typically have their own isolated power conversion circuitry. In many cases these analog circuits draw far less power than their digital counterparts. They can be regulated

with low-profile, integrated linear regulator packages which are not appropriate for processor chips.

Power Deregulation builds on two increasingly-common technologies: (1) dynamic frequency scaling and (2) chip-level multiprocessing. The following sections describe how these contribute to our scheme.

3.1 Dynamic Power-Performance Tradeoffs

Deregulated systems take advantage of dynamic frequency scaling (DFS), adapting the processor and operating system to the voltage of the battery instead of using dedicated hardware to control voltage. Although deregulated systems give up the energy efficiency benefits of manipulating voltage level, i.e., DVFS, they do not suffer the conversion inefficiencies of voltage regulators. Deregulated systems benefit from quadratic power improvements as battery voltage naturally decreases. Furthermore, recent work on adaptive resource sizing [15, 16] is compatible with deregulation and can offer further power reduction without the need of DVFS. Our simulation results indicate that the energy efficiency benefits of eliminating voltage regulation hardware frequently offset the energy efficiency disadvantages of forsaking explicit control over processor voltage.

3.2 Chip Multiprocessors

CMPs offer energy efficiency benefits over uniprocessors. They are already common in general-purpose and embedded computing applications. CMPs are especially suitable for applications with substantial thread-level parallelism, e.g., many multimedia consumer electronics applications. The popular Apple iPod already contains two ARM 7TDMI processors and its software is programmed to use multiple threads. Power Deregulation requires applications exhibiting thread-level parallelism. Given industry trends in consumer electronics and processor architectures, we believe systems and applications appropriate for Power Deregulation will be increasingly common in the future.

3.3 Frequency Scaling and Sleep Mode

At some points during the lifetime of the battery, we can expect the operating voltage to permit a higher frequency of operation than is required for the number of active processors. In these situations, frequency reduction or the use of periodic sleep modes can be used to permit reduction in power consumption while still meeting performance constraints; in this work, we assume periodically entering a low-power sleep mode, e.g., an fixed-rate MPEG codec may periodically encodes multiple frames and then sleep for a short period of time. Sleep modes are valuable because they can reduce static power in addition to dynamic power.

3.4 Reliability

It might at first appear that eliminating voltage regulators will render processors susceptible to additional reliability problems. In this section, we examine the impact of Power Deregulation on reliability.

1. **Long time scale degradation in battery voltage.** Battery output voltage changes at a rate on the order of 0.5 mV/s. As a result, setting the voltage at which frequency change occurs even slightly above the minimal value gives the operating system minutes to preemptively adjust frequency and the number of active cores.

2. **I–R drop as a result of changing processor power consumption and hence resistance.** The resistance between power and ground resulting from a processor changes as a function of switching activity, frequency, and voltage. Batteries and off-chip power delivery networks have parasitic resistance. This could potentially lead to changes in processor voltage, thereby reducing reliability.

Changes in processor resistance as a result of activating additional cores or changing frequency poses no difficulty because they can be explicitly considered when determining the mapping from battery voltage to processor frequency. However, changes in processor resistance as a result of changing switching activity due to instruction mix heterogeneity, pipeline effects, and cache effects at a particular voltage level must be carefully considered.

Let us consider a fairly conservative case: a nominally 624 MHz, 1.55 V XScale PXA270 processor. The minimum and maximum currents indicated in the datasheet [17] are 52.8 mA at 13 MHz and 597 mA at 625 MHz, yielding maximum and minimum resistances of 16.3 Ω and 2.60 Ω. The power delivery network between a voltage regulator and a processor clearly does not have sufficient series parasitic resistance to cause incorrect operation, otherwise the system would fail even with a voltage regulator. We therefore focus our attention on the series parasitic resistance of the battery. Lithium and alkaline AA cells each typically have internal resistances of less than 150 mΩ and a nominal voltage of 1.5 V. Therefore, even under these conservative assumptions, the maximum voltage across the processor changes by at most 68.1 mV as a result of changes to computation power consumption. This is well within the voltage variation tolerance of 410 mV.

3. **dI/dt effects.** The severity of dI/dt effects depends on the power delivery network between a voltage regulator and processor. Although Power Deregulation removes the power conversion circuitry, it does not worsen processor dI/dt effects for two reasons. First, the most critical impedance in the system is the *LC* tank formed by the chip capacitance and the package inductance. In a conventional system, this is a "near processor" phenomenon that a voltage regulator cannot mitigate because (a) it is electrically distant (i.e., the voltage regulator is on the wrong side of the nettlesome package inductance) and (b) the voltage regulator has a slow response, typically in the 1–10 kHz range [18]. The problematic resonance peak is often in the 10–100 MHz range. Additional capacitors placed on chip and within the package are the most effective ways of dealing with inductive noise [18]. We do not propose to eliminate them. Second, the dominant impedances in batteries are capacitive, not inductive [19], i.e., their inductance is dampened by very large intrinsic capacitance. In short, removing the power conversion circuitry is unlikely to worsen already-present dI/dt effects or introduce new ones.

From this analysis, it appears that Power Deregulation will not introduce additional reliability problems.

4. METHODOLOGY

This section describes our simulation environment, power model, and the benchmarks used for evaluating the proposed Power Deregulation technique.

4.1 Simulation Environment

We use the M5 multiprocessor simulator [20]. It has been configured to model the DEC Alpha 21164 (EV5) [21] and augmented with power models derived from Wattch [22]. Although M5 has not traditionally been used in the embedded systems domain, there are few other simulators that model chip multiprocessors running unmodified binaries including operating systems and representative multithreaded application workloads. We considered it important to determine the performance and power consumption of real multithreaded programs in the presence of non-ideal aspects of parallelism when evaluating the proposed technique. In order to better model an embedded chip multiprocessor, we configured the simulator performance and power models to correspond to a pipelined in-order processor rather than an aggressive out-of-order processor that M5/Wattch normally model.

While processors implementing the Alpha architecture have been most commonly used in high-performance systems, the basic instruction set architecture is similar to RISC architectures used in low-power embedded systems (e.g., the ARM instruction set).

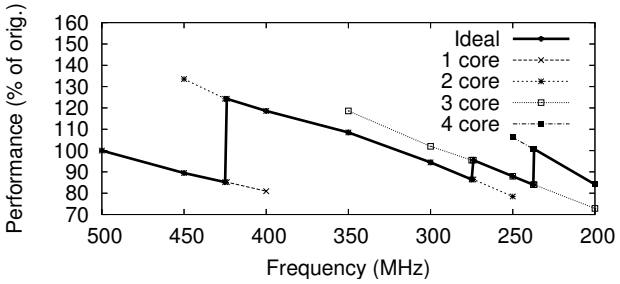

Figure 4: Relative performance for MPEG-2 decoding.

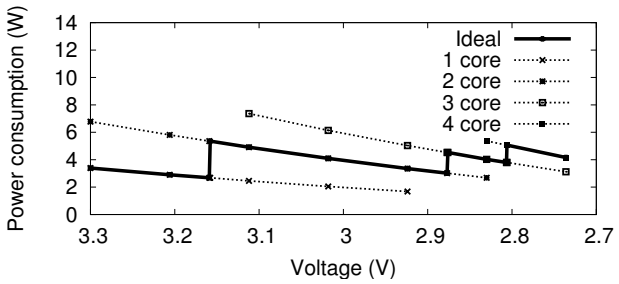

Figure 5: Power consumption of MPGdec based on transition points in Figure 4.

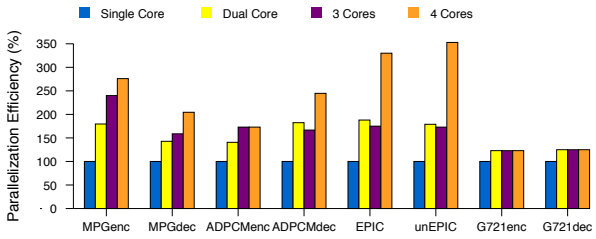

Figure 6: Parallelization efficiency of benchmarks.

M5 supports two different simulation modes: simple and detailed. The simple mode supports instruction-level functional simulation and the detailed mode supports cycle-accurate simulation. Our simulation methodology used a hybrid of these modes. We collected performance and power results for representative program phases and configurations using the detailed simulation mode. To compute whole-program execution times, we multiplied by instruction count data collected using the faster simple simulation mode. We collected processor power consumption values for frequencies ranging from 200 MHz to 500 MHz at intervals of 50 MHz. We jointly evaluate our processor and battery models over the lifespan of the battery, during which the battery voltage, and therefore processor frequency, gradually decrease. At each time instant, power consumption and performance values matching the current battery voltage are used.

4.2 Power Modeling

Our baseline architecture is an Alpha 21164 processor with a nominal V_{DD} of 3.3 V at 500 MHz. When Power Deregulation is used, battery voltage determines processor voltage, which in turn constrains frequency:

$$f = k(V_{DD} - V_{th})^a / V_{DD} \quad (1)$$

We model the effects a discharging battery would have on processor voltage and hence frequency. In addition, we use well-known equations to model the impact of decreasing voltage and frequency on both dynamic and static processor power consumption. Deregulated systems vary the number of active processor cores over time. Our power and performance models track the impact of activating additional computational resources. In addition, the use of sleep mode also impacts power consumption. Our results account for this by allowing processors to enter sleep mode when their natural performance exceeds the level required by an application due to discontinuities in performance resulting from the activation of additional processors.

M5 runs Alpha binaries on an unmodified Linux kernel. Consequently, we are currently restricted to using multithreaded benchmarks that were portable enough to be built for the Alpha architecture using a gcc cross compiler. We were able to compile a subset of the ALPBench [23] and MediaBench [24] suites. MSSG MPEG-2 encoder and decoder [25] (MPGenc and MPGdec) from ALPBench [26] are multithreaded applications that benefit greatly from additional processor cores. On the other hand, some of the MediaBench applications benefit less from additional cores, e.g., G721 voice compression, EPIC image compression, and ADPCM.

5. EXPERIMENTAL RESULTS

This section describes the evaluation of the performance and power consumption impacts of Power Deregulation.

5.1 Performance Evaluation

Figure 4 shows the relative performance of the MPEG decoding benchmark (MPGdec) at several frequencies. The lighter lines represent the impact of decreasing frequency on performance for a constant number of processors. Power Deregulation activates additional processors when the performance drops below a threshold, it has the effect of incrementally activating processors as battery voltage declines. The "ideal" curves in Figures 4 and 5 illustrate this trend. These figures indicate that performance gains from adding processors are non-uniform; the incremental gain from an additional processor depends on the application and the number processors that are already available. Note that both regulated and deregulated systems maintain the same levels of performance.

5.2 Impact on Overall Power Dissipation

Figure 5 shows the variation of power consumption during the lifetime of the battery. The "ideal" curve follows a saw-tooth pattern similar to Figure 4. One important difference is that the power cost of stepping up the number of cores is predictable while the performance benefit of enabling additional cores is irregular. This is due largely to the parallelization efficiency of the algorithms on the available number of processor cores. Figure 6 illustrates parallelization efficiency for all benchmarks running on one to four cores. Some benchmarks, including MPGenc, EPIC, and unEPIC have high efficiencies for four-core configurations. Other benchmarks, including MPGdec, ADPCMenc, and G721enc/dec have lower efficiencies. We will illustrate this concept via a comparison between two benchmarks: MPGenc and MPGdec. Figure 7 illustrates the impact of decreasing voltage and frequency, and compensating by increasing the number of active processors, on performance per Watt. The y-axis shows the performance per Watt normalized to the value at 3.3 V. This figure indicates that MPGenc gets more benefit from additional processor cores than MPGdec.

Note that when current voltage and number of processors permit a performance exceeding the required level, sleep mode is used to reduce power consumption while still meeting performance requirements. Many of our target applications are fixed-rate media processing programs. We can therefore transition to a sleep mode as soon as all the tasks for the next deadline have been completed. In Figure 8, we plot power consumption adjusted for use of sleep modes. The average power consumption is nearly constant for MPGenc due to its ability to exploit additional cores. In contrast, the

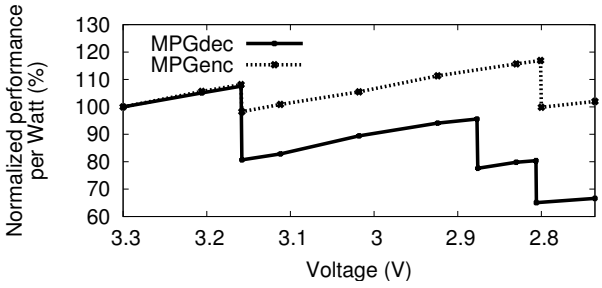

Figure 7: Relative performance per Watt.

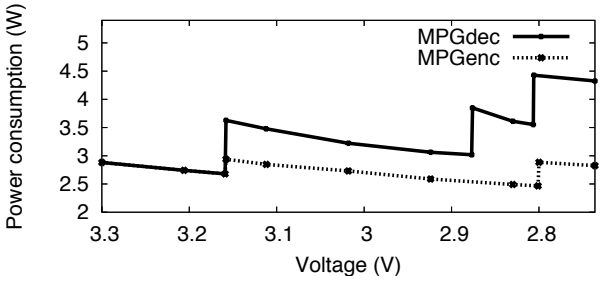

Figure 8: Total power consumption using sleep mode.

power consumption of MPGdec sometimes increases when additional cores are activated as a result of its poorer parallelization efficiency.

5.3 Battery Lifespan

This section compares the battery lifespan of a conventional regulated system and a system using the proposed technique. We have built a power consumption dependent time marching battery voltage simulator based on the discharge curves in the literature for a number of battery technologies, including lithium, lithium ion, liquid organic, and nickel-metal hydride batteries [27, 28]. Specifically, our models predict output battery voltage as a function of time under a time-varying current load. As the load drains the battery, the output voltage is decreased following the discharge curves in [27] until the battery reaches its cutoff voltage and can no longer supply energy. We use these models to evaluate battery lifetime and the energy-efficiency of Power Deregulation. For the regulated system, we assumed 85% conversion efficiency [1]. Figure 9 shows the battery discharge curves resulting from MPGenc and MPGdec benchmarks running on both regulated and Power Deregulated systems when a lithium battery is used. Power Deregulation substantially improves the battery lifespan of the MPEGdec application. The battery lifespan for MPGdec is not significantly affected by Power Deregulation. Note that the deregulated system has considerably lower bulk, weight, and PCB area. Whether Power Deregulation increases or decreases battery lifespan depends on the match between battery technology discharge curve and processor operating voltage range.

The effectiveness of Power Deregulation depends on the parallelism efficiency of applications. The main difference between the two applications shown, MPGdec and MPGenc, is the amount of performance gained when the second processor is activated. Figure 6 shows that MPGenc has a 174% boost in parallelism efficiency when the second processor is activated while MPGdec only gained 143%. Figure 10 illustrates the voltage discharge curves for the two applications running on an $LiMnO_2$ battery as a function of time. This figure shows that this influences the amount of energy consumed after the second processor is enabled, which determines to time required for performance to drops to 85%, requiring that the

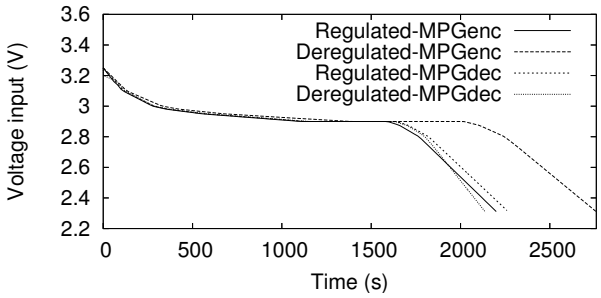

Figure 9: Voltage curves for $LiMnO_2$ battery.

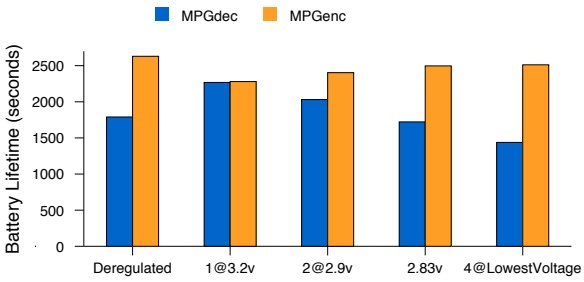

Figure 10: Battery lifetime comparison for MPGenc and MPGdec for both deregulated and various regulated systems with buck-boost converters for $LiMnO_2$ battery.

third processor be enabled. At 2.8 V, MPGdec requires three processors in order to meet performance requirements while MPGenc requires only two. This explains why MPGenc can operate longer than MPEGdec when using the same type of battery.

Table 1 compares the battery lifetimes of a Power Deregulated system with two types of regulated systems: one with a buck-boost converter and another with a buck converter. We use 85% conversion efficiency [1] for dedicated regulators. The minimum buck-boost input voltage is 0.8 V, enabling full use of battery energy. In our work, we assume that the processors can only operate within an input voltage range of 3.3 V to 2.55 V.

A system using a buck converter or Power Deregulated can only extract from 30% to 85% of the battery energy before reaching the minimum processor voltage, depending on the battery technology. Numerous battery technologies are considered, the discharge curves for which are shown in Figure 11. The effectiveness of Power Deregulation depends on the discharge curve of the battery technology in use. When a battery technology has a plateau in its discharge curve and the deregulated system has high performance per Watt at the plateau voltage, it will tend to outperform both buck and buck-boost regulation. For the batteries in Table 1 and Figure 11, we used the same energy quantity for each battery technology and the highest four lifetimes were all achieved with Power Deregulation. This implies that, given the ability to select a battery technology with an appropriate discharge curve, Power Deregulation has the potential to increase battery lifespan over buck-boost conversion in addition to permitting more compact embedded systems. Power Deregulation outperformed buck converters in all cases. However, Power Deregulation can only permit long battery lifespans when the operating voltage range of the processor is well-matched with the discharge curve of the battery.

6. CONCLUSION AND FUTURE WORK

Power Deregulation eliminates dedicated voltage regulation circuitry. It reduces frequency to compensate for decreasing battery

Table 1: Battery Life Simulation Results for MPGenc

Battery Technology	Li/MnO_2	$LiNiO_2$	$C/LiCoO_2$	$LiAl/MnO_2$	Li/MoS_2	NiMH
Voltage Supply Range (V)	3.25–2.3	4.25–2.9	4.0–3.15	3.05–1.85	4.5–2.5	2.76–1.84
Critical Region at (V)	2.9	3.95	linear	2.5	linear	2.56
Battery Life for Deregulated System (s)	2630	2553	2560	1178	2620	2374
Battery Life for Regulated System with buck-boost (s)	2512	2520	2503	2510	2203	2520
Battery Life for Regulated System with buck (s)	2301	2407	2503	1009	2196	2018

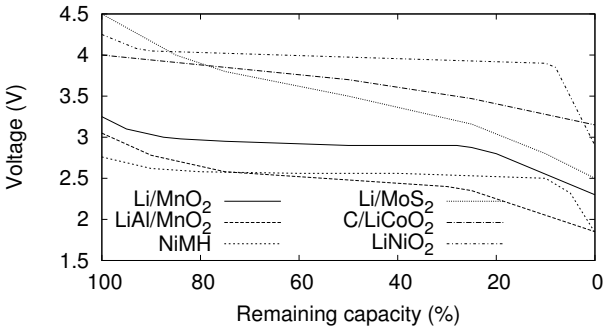

Figure 11: Discharge curves for different battery technologies.

voltage and activates additional processor cores to maintain required performance. It is most appropriate for battery-powered, multiprocessor systems running multithreaded or multiprogrammed applications, e.g., multimedia consumer electronics. Power Deregulation reduces PCB area by approximately 30% and eliminates potentially unreliable components such as electrolytic capacitors. Detailed multiprocessor and battery simulation indicates that Power Deregulation generally maintains similar battery lifespans to conventional regulated systems when both honor the same performance constraints.

7. ACKNOWLEDGMENTS

We would like to acknowledge David Brooks for early discussions that led to this work.

8. REFERENCES

[1] Linear Technology, *LTC3713 Low Input Voltage, High Power, No R^{TM}_{SENSE} Synchronous Buck DC/DC Controller*.

[2] M. Singer, "PCs plagued by bad capacitors," *CNET News.com*, Nov. 2005.

[3] B. Cole, "Tools help harness multicore power," *EE Times*, July 2005.

[4] G. Qu and M. Potkonjak, "Energy minimization with quality of service," in *Proc. Int. Symp. Low Power Electronics & Design*, Aug. 2000, pp. 43–49.

[5] M. C. Johnson and K. Roy, "Datapath scheduling with multiple supply voltages and level converters," *ACM Trans. Design Automation Electronic Systems*, vol. 2, no. 3, pp. 227–248, 1997.

[6] J. Chang and M. Pedram, "Energy minimization using multiple supply voltages," in *Proc. Int. Symp. Low Power Electronics & Design*, Aug. 1996, pp. 157–162.

[7] S. Raje and M. Sarrafzadeh, "Variable voltage scheduling," in *Proc. Int. Symp. Low Power Electronics & Design*, Aug. 1995, pp. 9–14.

[8] M. Schmitz and B. M. Al-Hashimi, "Considering power variations of DVS processing elements for energy minimization in distributed systems," in *Proc. Int. Symp. System Synthesis*, Nov. 2001.

[9] Crossbow, *MPR-MIB User's Manual*, June 2006.

[10] J. Polastre, R. Szewczyk, and D. Culler, "Telos: enabling ultra-low power wireless research," in *Proc. Int. Symp. Information Processing in Sensor Networks*, Apr. 2005.

[11] *MSP430x1xx Family User's Guide*, 2006, http://focus.ti.com.

[12] J. Luo, L.-S. Peh, and N. K. Jha, "Simultaneous dynamic voltage scaling of processors and communication links in real-time distributed embedded systems," in *Proc. Design, Automation & Test in Europe Conf.*, Mar. 2003.

[13] T. Pering, T. Burd, and R. Brodersen, "The simulation and evaluation of dynamic voltage scaling algorithms," in *Proc. Int. Symp. Low Power Electronics & Design*, Aug. 1998, pp. 76–81.

[14] Atmel Inc., *Atmel AVR ATmega128 Microcontroller User's Datasheet*, 2004, http://www.atmel.com.

[15] D. H. Albonesi, et al., "Dynamically tuning processor resources with adaptive processing," *IEEE Computer*, vol. 36, no. 12, pp. 49–58, Dec. 2003.

[16] R. Sasanka, C. J. Hughes, and S. V. Adve, "Joint local and global hardware adaptations for energy," in *Proceedings of the 10th International Conference on Architectural Support for Programming Languages and Operating Systems*, October 2002.

[17] *Intel*, Feb. 2002, http://www.intel.com.

[18] L. D. Smith, et al., "Power distribution system design methodology and capacitor selection for modern CMOS technology," *IEEE Transactions on Advanced Packaging*, vol. 22, no. 3, pp. 284–291, Aug. 1999.

[19] M. C. Glass, "Battery electrochemical nonlinear/dynamic SPICE model," in *Proc. Energy Conversion Engineering Conference*, Aug. 1996, pp. 292–297.

[20] A. G. Saidi, et al., "Performance validation of network-intensive workloads on a full-system simulator," University of Michigan, Tech. Rep., 2005.

[21] *Alpha 21164 Microprocessor: Hardware Reference Manual*, Digital Equipment Corporation, August 1998. [Online]. Available: http://diital.com/semiconductor/alpha/alpha.html

[22] D. Brooks, V. Tiwari, and M. Martonosi, "Wattch: A framework for architectural-level power analysis and optimizations," in *Proceedings of the 27th International Symposium on Computer Architecture (ISCA-27)*, June 2000.

[23] M.-L. Li, et al., "The ALPbench benchmark suite for complex multimedia applications," in *Int. Symp. Workload Characterization*, Oct. 2005.

[24] C. Lee, M. Potkonjak, and W. H. M. Smith, "Mediabench: A tool for evaluating and synthesizing multimedia and communications systems," http://cares.icsl.ucla.edu/MediaBench.

[25] "MSSG MPEG2 encoder and decoder," MPEG Software Simulation Group, 1994. [Online]. Available: http://www.mpeg.org/MPEG/MSSG/

[26] M. Li, et al., "ALP: Efficient support for all levels of parallelism for complex media," University of Illinois at Urbana-Champaign, Tech. Rep., July 2005.

[27] D. Linden, *Handbook of Batteries*, 2nd ed. McGraw-Hill Book Company, NY, 1995.

[28] C. A. Vincent and B. Scrosati, *Modern Batteries*, 2nd ed. John Wiley & Sons, England, 1997.