

## Invited Talk

# Techniques for Code and Data Management in the Local Stores of the Cell Processor

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### Abstract

The Cell Broadband Engine (CBE) contains one conventional PowerPC core with a standard cache hierarchy and eight Synergistic Processing Elements (SPEs), each of which contains a fast but small Local Store. These Local Stores are similar to ScratchPad memories, in that they are small, fast and directly addressed, but an additional constraint on programming the SPEs is that all Load/Store and instruction fetch accesses from the processor reference only the local stores. Access to the rest of the memory on a CBE system must be explicitly programmed using DMA commands. Techniques for fitting programs with large text and data footprints into the Local Stores, both manual and automatic will be described.

**Categories & Subject Descriptors:** D.3.3 [Programming Languages]: Compilers; C.1.3 [Other Architecture Styles]: Heterogeneous systems; C.1.4 [Parallel Architectures]

**General Terms:** Performance, Design, Experimentation, Languages.

### Bio

Mr. O'Brien has spent the last 26 years at IBM working in the fields of compilation and architecture. Initially, at the IBM Toronto Lab, he was the architect of the TOBEY optimizing back end (used in IBM's xlc, xlf, and xlc compiler products). Since then, he has spent 19 years at IBM Research, where his research interests have included multithreaded architecture, Smalltalk, Java, continuous optimization, binary translation, parallelization, and vectorization for several processors, most recently the Cell Broadband Engine. Mr. O'Brien received a B.Sc. degree in theoretical Physics and an M.Sc. degree in astrophysics from the University of London, Queen Mary College in 1974 and 1976 respectively. Currently he is investigating memory-related optimizations and parallelization for the Cell processor.