A 3D Timing Driven Placement Tool
Considering Placement and Timing of Interchip Vias

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Abstract
We focus on the placement of interchip vias in 3D integrated circuits using a force directed placement method. Static timing analysis is used in the inner loop of our placement tool to control timing.

Basics of 3D Force Directed Placement

Force directed placement is a well-known algorithm for placing cells or modules. In our 3D standard-cell approach we consider standard-cells to be cuboids having identical height and depth and different width. In general there are two forces applied to movable cells. One of them is an attracting force which is generated by connections between cells. The second force is applied to regularly distribute the cells over the layout volume. The vertical interconnections or so called interchip vias (ICVs) are considered during placement. Depending on the vertical distance of the standard cells, ICVs are added to the netlist. After the insertion of ICVs the placement is carried on for some iterations until the placement is checked whether ICVs can be deleted or whether new ICVs must be added. Since we consider a fully CMOS compatible technology, active elements must not be placed at ICV-positions. We assume vertical interconnects have the same z-dimension as standard-cells. The ICVs are placed along with the standard-cells, width and height of the ICV-cells rely on technology parameters.

Integrated Timing Analysis Considering ICVs

Our placement tool follows the approach to control the circuit's timing already during placement. Therefore, we integrated a static timing analysis (STA) in the inner loop of the placer. We apply an additional force that considers the results of the STA. This force is a path force which directly uses timing to influence the placement. In contrast, common standard force directed placement methods are based essentially on a wirelength metric, while timing is not considered. We use the Elmore Delay for modelling the delay of the interconnects. The vertical interconnects are especially considered. An ICV is modelled as a piece of

interconnect with different resistance and capacitance values. These values can be adjusted to the applied technology.
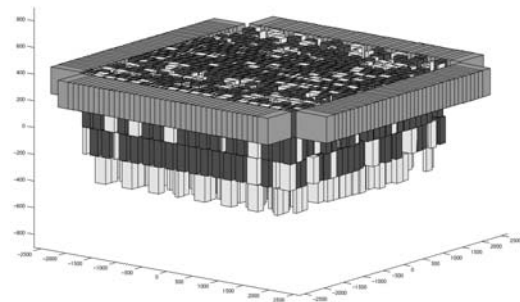

Figure 1: 3D placement example

Results

Figure 1 shows a 3D placement result of our placement tool, placing ICVs and using the integrated STA. Standard cells are bright, ICVs dark. Figure 2 shows the 25 most critical paths for two different placement runs of a benchmark circuit. The first run was done without path forces. The second run applies path forces, which consider the STA results to improve timing. Negative slack is eliminated, timing constrains for the placement are met.
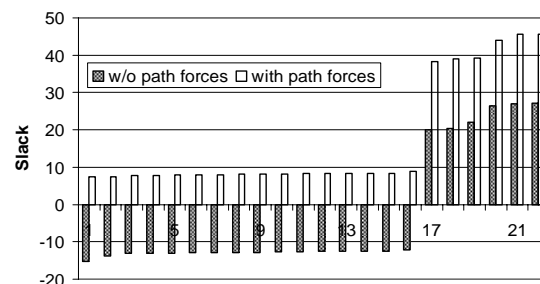
Figure 2: Slack of the 25 most critical paths