DefSim – the defective IC

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http://www.defsim.com

Abstract

With DefSim you can study behaviour of physical defects in digital circuits. The kit consists of a chip (with >500 defects), a measurement box and software, representing a unique research environment.

1. Introduction

Accurate fault and defect modeling for current technologies represent an important challenge for both the semiconductor industry and academia. At the same time, accurate electric simulation on the layout level became nowadays a big challenge, due to growing impact of process variation and other phenomena in modern semiconductor technologies. As the result, in many cases, the electrical simulation results do not match with the reality. Hence, they cannot be reliably used for developing and evaluating new test methodologies and fault models. Experimental study and understanding electrical level phenomena produced by *real* physical defects and their reflection on the logic level in terms of logic signals becomes, therefore, an important instrument for researchers and educators.

The newly developed experimental and measurement kit called *DefSim* facilitates the study of physical defects and their influence on the operation of digital circuits. It can be used as a first step to understanding the real behavior of physical defects and evaluating newly developed fault models and testing methodologies for modern electronics. The central element of the DefSim kit is an integrated circuit (IC) with more than 500 various defects physically injected into a set of digital standard cells and small circuits. The IC is attached to a dedicated measurement box (see Figure 1) serving as an interface to the computer. The measurement box supports two measurement modes – voltage and I_{DDQ} testing [1]. The communication between the DefSim hardware and software goes through the standard USB port.

Figure 1: DefSim chip on its measurement box

2. DefSim IC Implementation

The DefSim IC has three main structural parts: a matrix of simple digital circuits, addressing mechanism, and a measurement circuitry [2]. Each circuit from the range is implemented in many copies where one of them is correct and all the others are intentionally defective. It is possible to select any defect of interest by addressing a corresponding copy of the circuit.

When a circuit and a defect are selected, the user can apply an arbitrary input test sequence and measure the circuit's response in terms of both the binary logic values and static supply current levels (I_{DDQ}). It is also possible to compare the behavior of the defective version to the correct copy of the same circuit.

Currently two types of defects are implemented in DefSim: opens and zero-resistive shorts in conducting layers like Polysilicon, Metal1, and Metal2. These defects are located both inside logic gates and upon (or between) signal lines outside the gates.

Before designing DefSim, a strong decision was made – defect implementation in the chip should be as much as possible close to the silicon reality. As the result, DefSim defects are fixed and have local (spot) features. It is also important that the overall initial layout of each circuit remained unchanged too. Moreover, each circuit under test is loaded and driven by standard non-inverting buffers. All these measures ensure that the implementation of defects is kept as close to silicon reality as possible.

The DefSim chip was designed in AMS 0.8µm CMOS (double-metal, double-poly) technology. The chip is composed of approx. 48000 transistors and occupies 19.90 mm^2 of silicon.

3. Working with DefSim

The DefSim software package provides a convenient access to the features of the IC and ensures a smooth way of performing various experiments. There are two different levels of the DefSim software are available: a stand-alone workstation version (Figure 2) and a server-based version (http://www.defsim.com). The first one is optimized for a

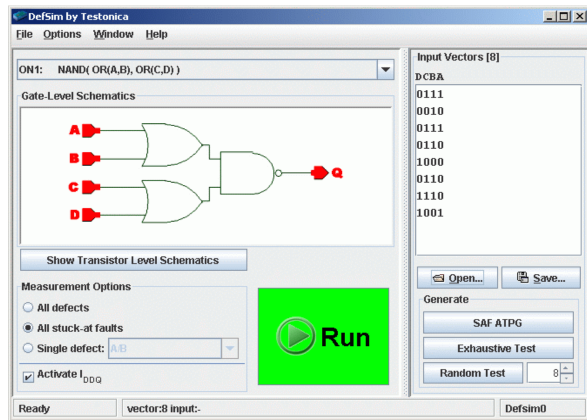

Figure 2: Graphical user interface of DefSim

quick start and personal use, while the second targets large groups of users. The server-based version also suits for organizing study process in classrooms, distance e-learning or remote Web-access services.

In both DefSim environments it is possible to observe the truth table of correct and defect circuits, obtain defect/fault tables for all specific defects, define test patterns automatically or manually, study behavior of bridging and open faults, etc. Since DefSim environment supports both voltage and I_{DDQ} testing, the user can compare the fault detection efficiency of those test methods as well.

A simple DefSim workflow scenario can be the following. As the first step, the user has to select a target circuit to work with. Then, the list of implemented defects for this circuit becomes available. The user can work either with a single specific defect or with a group of defects simultaneously. Besides the fault list, two types of schematics are available for each circuit: the logic level scheme and transistor level one. The necessary test patterns can be generated either by the user using these schematics or automatically by the software.

Then, the prepared test patterns are sent to the IC and applied to either the selected defect or a group of defects, and consequently, the circuit responses are recorded. The results of measurements are displayed in several different forms. For instance, the user can observe the truth table for a certain defect, or a defect table for a group of defects, or I_{DDQ} value info. The resulting test data can be stored for later retrieval and modification.

Typical DefSim-based exercises include the following:

- test generation for opens in a small circuit using a transistor-level schematic and in a bigger circuit using a logic-level schematic;
- finding all possible test vectors for a given short and calculation of its truth table;
- checking the efficiency of SAF test in detection of shorts and opens;
- detection and localization of an unknown defect;
- study different fault models and compare them
- study of shorts that form memory elements inside combinational circuits.

A bit more advanced exercises are considered in [3, 4].

4. Conclusion

In this project we have developed a complete solution for experimenting with the influence of most common CMOS defect types: opens and shorts. These defects are physically implemented in silicon and represent a trustworthy source of different phenomena similar to those appearing in defective VLSI chips. The developed IC allows applying both voltage (i.e. logical) and current test methods and offers comparing of their efficiencies on basic of digital circuit examples.

The DefSim IC comes with a dedicated "plug-and-play" measurement box and handy software that provides a flawless work for both individual users and large groups of students. The whole DefSim bundle represents a unique and easy to handle research and educational environment.

5. References

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Slovak University of Technology (FEI STU) – research work and BICM for IDDQ testing.

Server software, graphical UI, package integration was performed by Testonica Lab (www.testonica.com).

The DefSim hardware was developed using software tools from Cadence Design Systems.

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