Demonstration for the DATE 07 University Booth
Monte Carlo Simulation with novel statistical Design Kit

Wolfgang Schneider, Dirk Eichel, Atmel Germany GmbH, Heilbronn
Michael Schröter, Holger Wittkopf, CEDIC TU-Dresden

Abstract

Optimal correlation with the statistics of the technological process and stat. models are in a design kit implemented. For yield optimisation in the early development phase new possibilities are opened.

1 Monte Carlo- and Corner-Simulation

In order to guarantee a high manufacturing yield and avoid redesigns in an early stage of the IC design flow, for a long time in the circuit development simulation tools are already used, which reproduce the effects of the inevitable parameter fluctuations of the manufacturing process. For the simulation of boundary conditions of the used process the corner simulation with defined worst case conditions is used. For the reproduction of the entire process statistics the Monte Carlo simulation is used. For digital CMOS circuits slow/fast combinations are usual corner cases. For analog circuits the spread of the different process parameters leads to a completely different behaviour of the respective circuit. With the designkit presented here a new way for the modelling of the statistic process variables was taken: Without detour over electrical characteristics (beta, Early voltage…) scalable models are generated with the help of the expert system TRADICA directly from the geometrical description and the process data and/or the process statistics. Components and electrical characteristics, which depend on the same technology parameters, maintain their correlations with the modelling. Without additional expenditure thereby also the statistic characteristics of these parameters in the model are implemented. A condition for it is a sufficiently large database. The PCM (Process control monitor) were evaluated which are several times on each produced wafer.

2 The Statististical Design Kit in praktical use

The demonstration shows the application of the Monte Carlo simulation at a simple circuit example. It shows the analysis of the minimisation of the DC offset of an operational amplifier.(fig. 1)

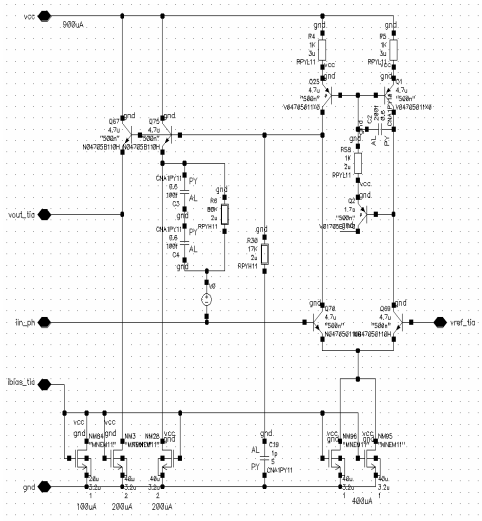

Figure 1 Circuit example fort the demonstration

Process parameters and mismatch of components can be simulated separately or together statistically. The result of the combined analysis gives directly the parameter dispersion which can be expected after the technological run.

The statistic simulation of the process variations makes views of correlation between process parameters (e.g. layer resistances, base diffusion etc.) and the interesting output characteristics for the circuit possible. Over the evaluation of the correlation coefficients those process parameters can be identified, which affect the circuit considerably. It will be now possible to define corner cases, which fit to the regarded circuit. Also the effect of individual process parameters is analyzable, for example in a sweep of process parameters.

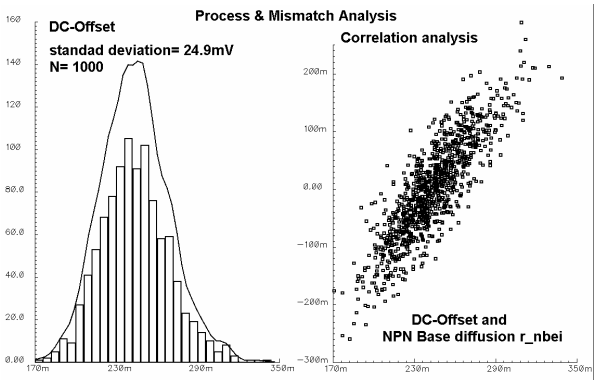

Figure 2 DC offset spread and correlation with NPN base doping r_nbei

The Mismatch analysis shows the dispersion of neighbouring elements. The geometrical dimensions with their characteristic dispersion are built in the designkit, which is determined from special PCM mismatch structures. Since at each element the mismatch Property is selectable, all elements can be simulated together or only selected elements alone statistically. The result of the Mismatch analysis leads to critical element dimensions. It is practically realizable however only with at the same time very carefully implemented IC layout. In the demonstration the example circuit is optimized gradually:

- by inserting a base current compensation
- Bufferstages give better decoupling
- Cascodestages increases the open loop Gain.

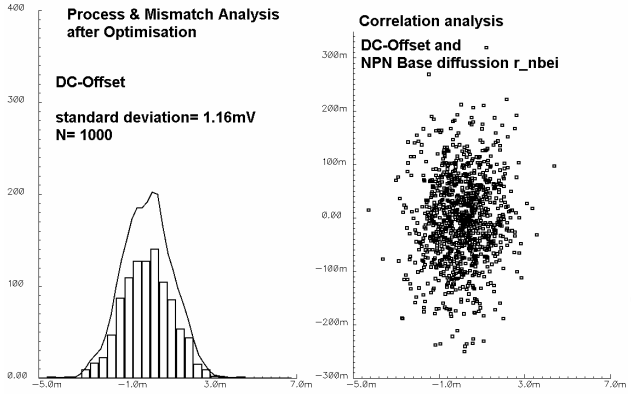

Figure 3 After the optimization the DC offset spread is minimized and its dependence on NPN base doping r_nbei disappeared

3 Practical Experiences

The presented procedure worked satisfactorily already several times at complex circuits and is applicable to all kinds of simulation (AC, transient, PSS…). The simulation fits usually good to the measured data.

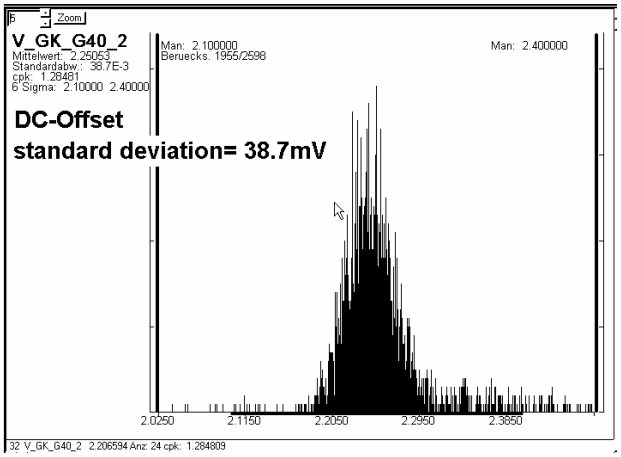

Figure 4 Measured offset spread of a complex amplifier stage

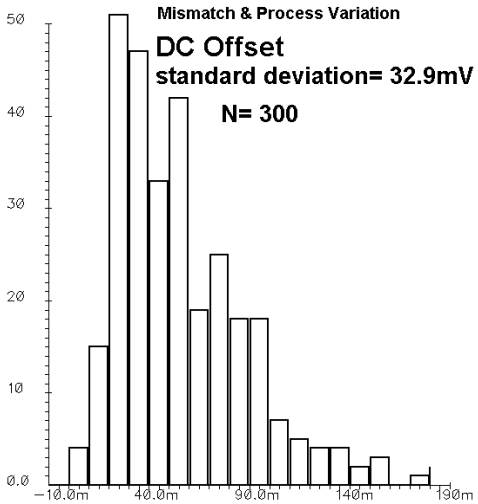

Figure 5 Results of the corresponding mismatch and process simulations

4 Literature

[1] Kraus, W.: PCM- and Physics-Based Statistical BJT Modeling Using HICUM and TRADICA, 6th HICUM Workshop, 2006

[2] Schröter, M., Wittkopf, H., Kraus, W.: Statistical modeling of high-frequency bipolar transistors, Proc. BCTM, pp 54 - 61, 2005