LEMOS Project

Low-Power Design Methods for Mobile Systems

http://lemos.offis.de

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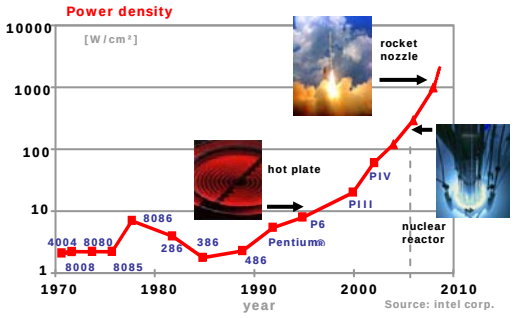
Abstract

In the German funded project LEMOS, new EDA techniques and methods are developed to drastically reduce power consumption of System-on-Chips (SoCs), leading to significant increase in design efficiency and productivity.

1. Introduction

The integration of a rapidly increasing number of highly complex tasks occupying minimum chip area is made possible by minimising the structural size of integrated circuits. The enormous amount of demanded computing power has in the past enabled new services and devices in particular in the mobile communication, automotive and computing market. This computing power is provided mostly by operations switching at ever higher frequency. Today, the physically induced power dissipation represents the limiting factor to a further increase of the capability of integrated circuits. Already, the power density of integrated circuits exceeds that of glowing hot plates (Fig. 1). Without significant improvements in design methods, power density would very soon reach the



level of a nuclear reactor or even of a rocket nozzle.

Figure 1: Increase of power density for x86-architecture

Hence, high power consumption is problematic in regard of heat dissipation as well as of energy supply. So, apart from economic aspects or reliability needs, the reduction of the power dissipation of integrated circuits additionally is of global ecological significance and therefore has to be taken into account early in the design process.

One inevitable means for handling the exponentially increasing design complexity is the Electronic Design Automation (EDA). EDA techniques and methods are essential especially for solving the problem of power dissipation.

2. Objectives

LEMOS [1] addresses the problem of power dissipation where the main objectives are:

- a significant increase in design efficiency and productivity,
- to move the limit to what has technically not been possible so far due to the problem of power dissipation,
- to decrease the number of power consumption-caused re-designs,
- reducing development time by more than a third,
- resulting in a drastic reduction of power consumption.

The product differentiation provided this way will be a substantial contribution to strengthen the competitive position of the German industry. In close cooperation with the partners Infineon Technologies AG and ChipVision Design Systems AG, further Nokia Research Center, Robert Bosch GmbH and Catena Software GmbH, e.g. methods for early estimation and especially optimization of the power consumption of embedded systems are developed and then integrated into the tools of the EDA partners.

The project, funded for a period of three years by the German BMBF (Bundesministerium für Bildung und Forschung), finished in March 2007 (grant no. 01M3155). The project executing organisation is the DLR (Deutsches Zentrum für Luft- und Raumfahrt e.V.) [2].

3. Results

As stated above, the main goal is a drastical increase in design productivity by avoiding redesigns necessary due to power dissipation. To achieve this goal, the scientific and technical objectives are threefold, dividing the project into three work packages: The research of methods for reduction of power dissipation, the integration of these methods into a power-aware EDA flow, and eventually the evaluation of the results in industrial design environment. In addition, research and development in LEMOS focuses on more abstract levels of design, providing even higher potential for optimization.

Algorithms and methods developed and assessed in the first work package are partitioned by the structures and components of the targeted system: busses, memories, analogue blocks, digital logic, RF front-ends, components for clock generation. Orthogonally to these, power management is addressed as well.

Generally, system composition, i.e. the architecture of the components, has to be adapted to the optimization methodology. As a consequence, circuitry measures have to be developed in order to make the components applicable for power management.

Examples of the results from LEMOS include optimizations accomplished by Infineon founding on multi-Vth libraries and a new design methodology resulting from the project. For a reference design, a reduction in power consumption of 94% was achieved, using newly designed low-leakage cells. In the domain of digital logic, a patent has been applied for by Infineon, enabling a new technique (Charge Recycling Circuit Block Switch-Off Scheme for Short Power-Down Periods) allowing power reduction up to a factor of 5000 for according structures [3] [4].

A rule-based approach for automatic synthesis and verification of clock gating at RT level was researched by Bosch, already successfully being integrated into the tools as well as into the design flow of Bosch.

Nokia developed a new fast flash AD converter, allowing higher resolution (8 bit) and sampling rate (1 GSPS) in a 65 nm process, providing higher robustness regarding supply voltage and temperature noise, and a multitude of new features, but consuming 10 to 20 times less power than the previous converters based on 130 nm process.

For early estimation and optimization at architectural level of power dissipated by bus interconnect, a new methodology was jointly researched by Bosch, Nokia, and ChipVision, accompanied by their subcontractors OFFIS and FH Pforzheim. The new approach allows power estimation for different encodings and protocols, based on newly developed models for interconnect and components, a prediction of the resulting geometry, also supporting differential on-chip communication systems.

The project partner Catena [5] with its subcontractor TU Cottbus developed new algorithms for partitioning, placement, layout, and constraint-driven routing, focussing on power reduction [6]. These algorithms have been integrated into the tools of Catena resulting in designs additionally showing area savings of more than 10%.

The high-level design methods evolved from LEMOS have been integrated into the design tools from the EDA vendor ChipVision, mainly the tool ORINOCO® DALE [7]. Now being integrated into the design-flow of the industrial partners, the tool allows power estimation and optimization at the Electronic System Level (ESL), at which the most significant reduction of energy consumption can be achieved (Fig. 2).

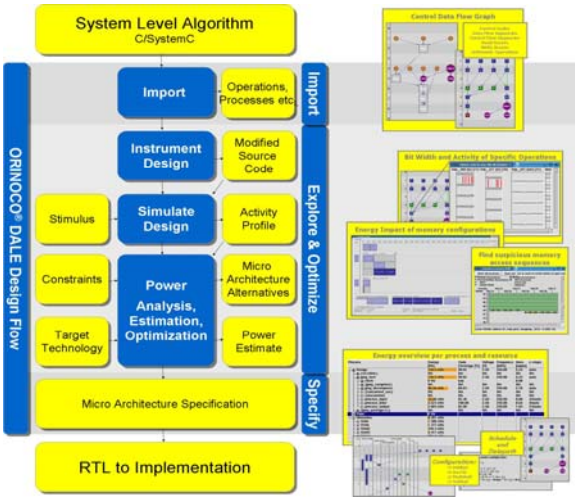


Figure 2: ESL power estimation and optimization flow

Eventually, the LEMOS methods and tools have been successfully evaluated based on several test-chips from Infineon and Bosch in order to prove the gain in power savings, now enabling new products.

4. Conclusions

Power consumption rapidly becomes a main show-stopper for new electronic products. One inevitable means for handling nowadays complexity are EDA techniques and tools. But existing methods and tools still lack of support for power estimation and optimization. To close this gap is the goal of LEMOS and ongoing research of the project partners.

References

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