Hyperion: A sensor node test bed for (high-speed) power measurements

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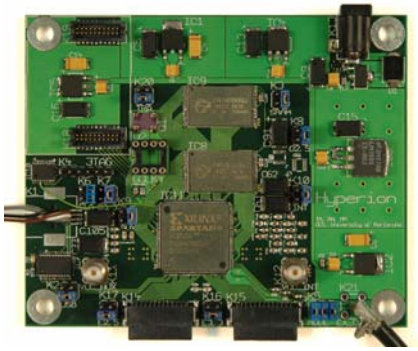

Figure 1: Hyperion sensor node

Abstract

The Hyperion platform, a measurement test bed for sensor network applications allows a power resolution that goes beyond the clock cycle i.e. currents that vary within a clock cycle can be captured.

1. Introduction

We present the Hyperion platform (Figure 1), a highly flexible test bed for sensor network applications. Its flexibility allows for designing sensor networks under varying architectural (both, software and hardware) constraints and therefore supports fast design space exploration. In addition to its flexibility, a distinctive feature of Hyperion is its capability to measure power/energy consumption of individual sensor node components (like radio, CPU, memory, sensors etc.) very accurately through a proprietary measurement infrastructure. As opposed to similar approaches [1] it actually allows a power/energy resolution that goes beyond the clock cycle i.e. currents that vary within a clock cycle can be captured / measured. We have experienced that in-cycle accuracy is mandatory in order to draw reliable conclusions for designing a low power/energy sensor node.

Advanced sensor networks equipped with demanding sensors such as the image sensors found in Hyperion require ample computational power. This will be the case for many sensor networks in the future. Since sensor nodes draw their energy from (re-chargeable) batteries and/or harvest energy from the environment (solar etc.) the power consumption is a crucial metric that determines their usability and deployment. A detailed energy consumption break-down is necessary to understand potential optimization opportunities in hard- and software. The obtained data is also essential for adjusting simulation model parameters needed for realistic assessment of the entire sensor network on a simulation level.

2. In-cycle accuracy measurements

As an example, for the in-cycle accuracy achievable by Hyperion, a series of "load word" instructions executed in a loop has been measured (Figure 2). The current waveform obtained, reveals large current spikes at the end and beginning – caused by the transition to the "jump" instruction at the loop body. Without these measurements such important findings would have gone unnoticed.

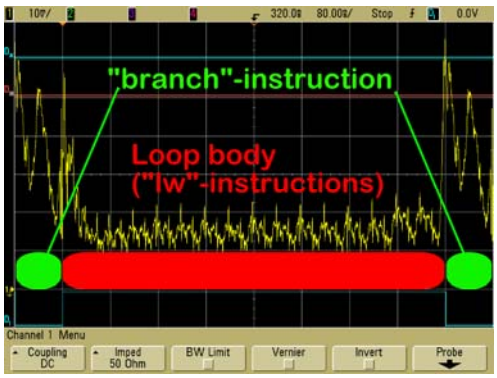

Figure 2: Loop power consumption (CPU)

Figure 3 shows the detailed power consumption of different MIPS instructions in the execution stage [2]. The measurement results can be used to evaluate different processor implementations and/or to instruct a compiler backend to schedule instructions accordingly. The designer has the freedom to direct data flows between these components: e.g. digitally sampled image data can be directly moved into the memory or to the radio – unmodified or (pre)processed depending on the design goals and/or available power.

3. Hyperion sensor node hardware

An FPGA (Field-programmable gate array) implements the sensor node hardware (various soft-core CPUs etc.) under evaluation and is the central connection point for all components. It interfaces with the memory (SRAM), a high resolution color image sensor (CMOS) and a freely programmable wireless transceiver.

4. Design of the in-cycle measurement infrastructure

During the design of the Hyperion measurement infrastructure special attention was paid to achieve an undistorted reading of the logic current drawn by the FPGA logic. To reveal the current waveform, a precision shunt was placed between the decoupling capacitor network and the FPGA. The precision shunts used are within the mΩ - range, exhibit very little inductance and are suitable for high current (pulse) measurements.

The current waveform is not accessible in standard boards because it is low pass filtered by the decoupling capacitors and layer capacitances.

Since the power- and ground layer capacitance below the FPGA cannot be physically moved like the capacitors, the area beneath the FPGA was left blank eliminating power plane capacitance.

To ensure high fidelity measurements, extensive SPICE simulations were conducted. Especially the decoupling capacitor network was designed for a flat impedance profile over a large frequency range reducing anti-resonance spikes to a minimum. The PCB (Printed Circuit Board) layout still keeps all decoupling capacitors within their effective ranges. Additionally, capacitor pads use a via-in-pad geometry to reduce parasitic inductances which also contributes to the flat impedance profile.

For power supply, linear voltage regulators are used. These cause the least signal distortions when compared to more power efficient solutions. Since Hyperion is primarily a test bed for design space exploration, efficiency in the power supply can be neglected. Power needs to be supplied by batteries to avoid high frequency spikes found in the main power supply. However, the overall power consumption is already quite low when compared to other FPGA based boards. The selected FPGA and the other (low-power) components (e.g. SRAM, CMOS camera sensor) draw very little power.

4. Conclusion

The Hyperion sensor node has proved that in-cycle accurate measurements are feasible if the PCB is meticulously designed for low capacitances and carefully selected components (e.g. shunts, low ESR-capacitors) are used. Simulation has been invaluable during the design of the decoupling capacitor network – especially for avoiding anti-resonance spikes in the impedance profile.

The findings of in-cycle accurate measurements are used to detect and optimize the hardware implemented by the FPGA.

In addition to the in-cycle measurements Hyperion's capability to assess the average power/energy consumption of individual sensor node components (like radio, CPU, memory, sensors etc.) is necessary for the optimizations on component/application level).

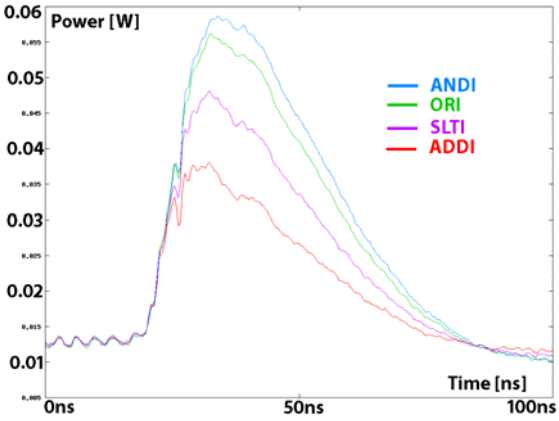

Figure 3: Power consumption of different MIPS instructions in the execution stage

5. References

[1] Geoff Werner-Allen, Pat Swieskowski, and Matt Welsh, "MoteLab: A Wireless Sensor Network Testbed", In Proceedings of the Fourth International Conference on Information Processing in Sensor Networks (IPSN'05), Special Track on Platform Tools and Design Methods for Network Embedded Sensors (SPOTS), April 2005.

[2] Plasma MIPS-Softcore (www.opencores.org)