MIXED-SIGNAL CLOCK-SKEW CALIBRATOR FOR TIME-INTERLEAVED ANALOG-TO-DIGITAL CONVERTERS

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Abstract

The clock-skew error in time-interleaved ADCs importantly degrades their linearity. Our demo shows an extremely simple mixed-signal clock-skew calibrator for this application.

1. Introduction

The clock-skew error in time-interleaved analog-to-digital converters (TI ADCs) importantly degrades the linearity of such converters [1]. This nearly constant but unknown error, that must not be confused with random jitter, prevent TI ADCs from perform uniform sampling. There are some different techniques of facing up the clock-skew error: two-ranks sample-and-hold [2], channel randomization [3], global passive sampling [4], clock-edge reassignment [5], all-digital calibration techniques [6] and all-analog calibration techniques [7]. We propose a new kind of mixed-signal clock-skew calibration technique, divided into two subsystems: a digital clock-skew detector and a digitally trimmable multi-phase sampling clock generator. Compared to the mentioned all-digital calibration techniques, ours distinguishes itself by the simplicity of its hardware elements. On the other hand, compared to the all-analog ones, ours keeps the inherent robustness of a digital clock-skew detection.

2. Overall description of the demonstrator

Fig. 1 shows a diagram of our demonstrator, a clock-skew calibrated two-channels TI ADC. It consists of two 10-bit commercial ADCs, a FPGA to implement the digital clock-skew detector subsystem (DDSS) and an ASIC in a CMOS 0.35 µm technology to implement the digitally trimmable multi-phase sampling clock generator (DTCG). The DDSS extracts from the multiplexed ADCs' outputs $y[n]$ a measure of the clock-skew affecting the sampling clock driving the ADC_1, Φ_1. Then, it tells the DTCG whether Φ_1 must be advanced or delayed with regard to the sampling clock reference, Φ_0, to obtain, neglecting random jitter, an uniform sampling. So, the DTCG converts the digital information provided by the DDSS in extra delays on the sampling clock paths. Both subsystems are embedded in a stable closed-loop, so the overall system has the potentiality of following the variations of the clock-skew error.

Due to the discrete nature of the elements used in the demonstrator, the sampling frequency of a single ADC is limited to 25 MHz. Besides, the actual clock-skew error is expected to be around a half nanosecond, i.e., two orders of magnitude higher than the error expected in a fully integrated TI ADC and sampling clock generator. However, a special effort has been made to attain a residual clock-skew of the order of one picosecond.

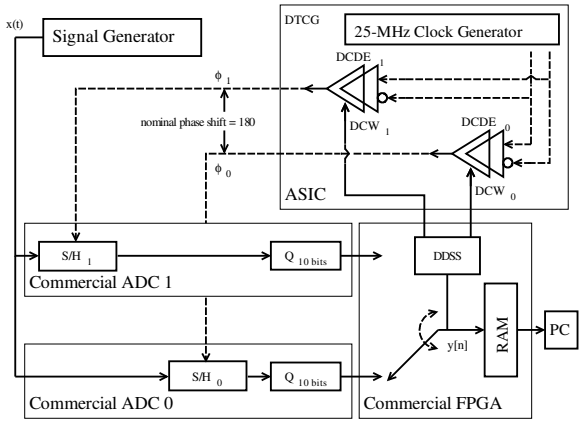

Figure 1: Diagram of our demonstrator for the mixed-signal clock-skew calibration technique

3. Digitally trimmable multi-phase sampling clock generator (DTCG)

The DTCG consist of a clock generator and two digitally controlled delay elements (DCDEs). The clock generator is a differential voltage controlled ring oscillator embedded in a phase-locked loop similar to that shown in [7]. A DCDE consist of a differential-to-single-ended converter (DTSEC) and a digitally trimmable bias generator (DTBG). Two differential clock signals, nominally shifted 180°, are single-ended converted by two DCDEs, becoming Φ_0 and Φ_1. At the same time, a delay $t_{cal\,i}$, $0 \le i \le 1$, can be added in any of the clock paths. This delay depends on the value of the digital control word DCW_i, $t_{cal\,i} = t_{step} \cdot DCW_i$, where t_{step} is the time step of this digital-to-time conversion. The delay $t_{cal\,i}$ gets modified by altering the operating point of the DTSEC. The residual clock-skew after calibration, t_{res}, is expected to verify $|t_{res}| \le t_{step}$.

There exists a linear relation between the bias voltage of the DTSEC, V_{bias}, and $t_{cal\,i}$. So prior to the voltage-to-time conversion, a digital-to-voltage conversion must be performed. It is done by means of the DTBG shown in fig. 2. The DTBG consist of a set of switchable current sources embedded in a bidirectional shift register, serial-in, parallel-out, of N static storage cells Q_j, $0 \le j \le N$. When Q_j is in high state, the associated current source is turned on injecting

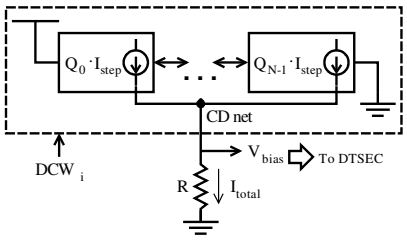

Figure 2: Diagram of the digitally trimmable bias generator

I_{step} in the common drain net CD net, and when it is in low state, the current source is turned off. The signal DCW_i modifies the state of the shift register. The overall current I_{total} gives a V_{bias} voltage by means of a resistor.

4. Digital clock-skew detector subsystem (DDSS)

Fig. 3 shows a diagram of the DDSS. Although our

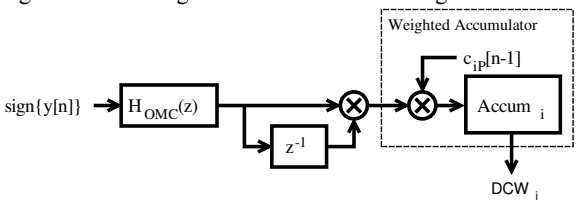

Figure 3: Diagram of the digital clock-skew detector subsystem

demonstrator is limited to a two-channels TI ADC, we show here the necessary elements for any number M of channels. The input signal is physically one bit carrying the sign information about $y[n]$. This greatly simplifies the required hardware and makes the DDSS robust against gain mismatch between channels. The transfer function of the digital filter $H_{OMC}(z)$ is $1\text{-}z^{-M}$, where *OMC* stands for offset mismatch cancellation. This filter is necessary to guarantee that the offset mismatch does not prevent the DDSS from properly working. The weighted accumulator modulates its input signal by the modulation signal $c_{iP}[n]$. This is a fixed periodic signal of integer numbers ranged from $-(M\text{-}1)$ to $M\text{-}1$ that depends on the Φ_i subscript of the sampling clock signal to be calibrated, for $1<i<M\text{-}1$ [8]. For the two-channels case, there is just one sampling clock to be calibrated, Φ_1, and one period of $c_{1P}[n]$ is simply [+1, -1].

5. Results

Fig. 4 shows the $y[n]$ spectrum from a measure before calibration. The low frequency signal is the desired output signal, i.e., the sampled input signal $x(t)$. The high frequency signal is the distorsion due to clock-skew when sampling $x(t)$. Our calibration technique reduces this spurious tone at the noise threshold level, greatly improving the spurious free dynamic range. The measured t_{step} is 1.5 ps with an uncertainty of about 30%.

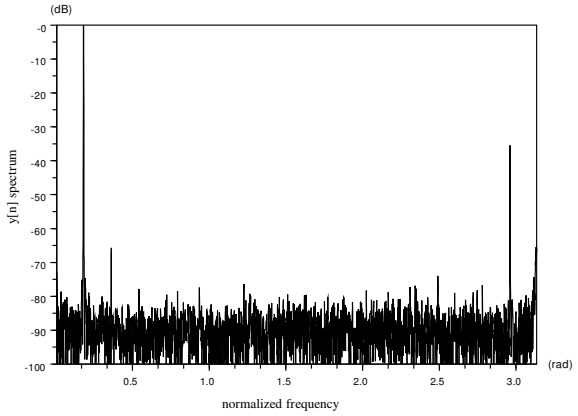

Figure 4: $y[n]$ spectrum before calibration

6. Conclusion

This demonstrator shows the feasability of our mixed-signal clock-skew calibration technique in a highly hostile environement of interconnected discrete components. However, this technique is intended for fully integrated TI ADCs, where the expected clock-skew is of the order of some picoseconds before calibration. It will be the aim of future developments.

7. References

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